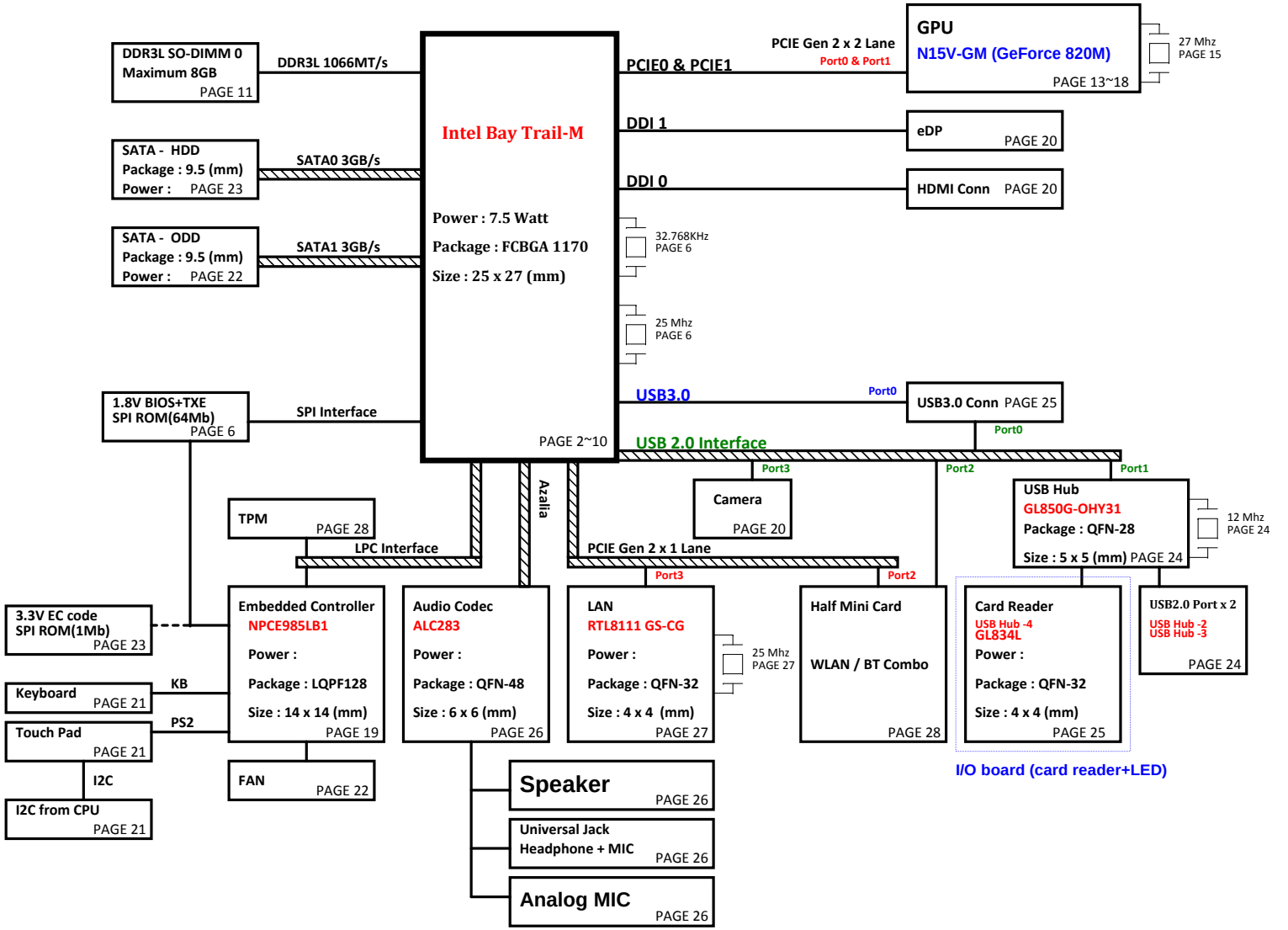
ZYL (17")
Intel Bay Trail-M Platform Block Diagram

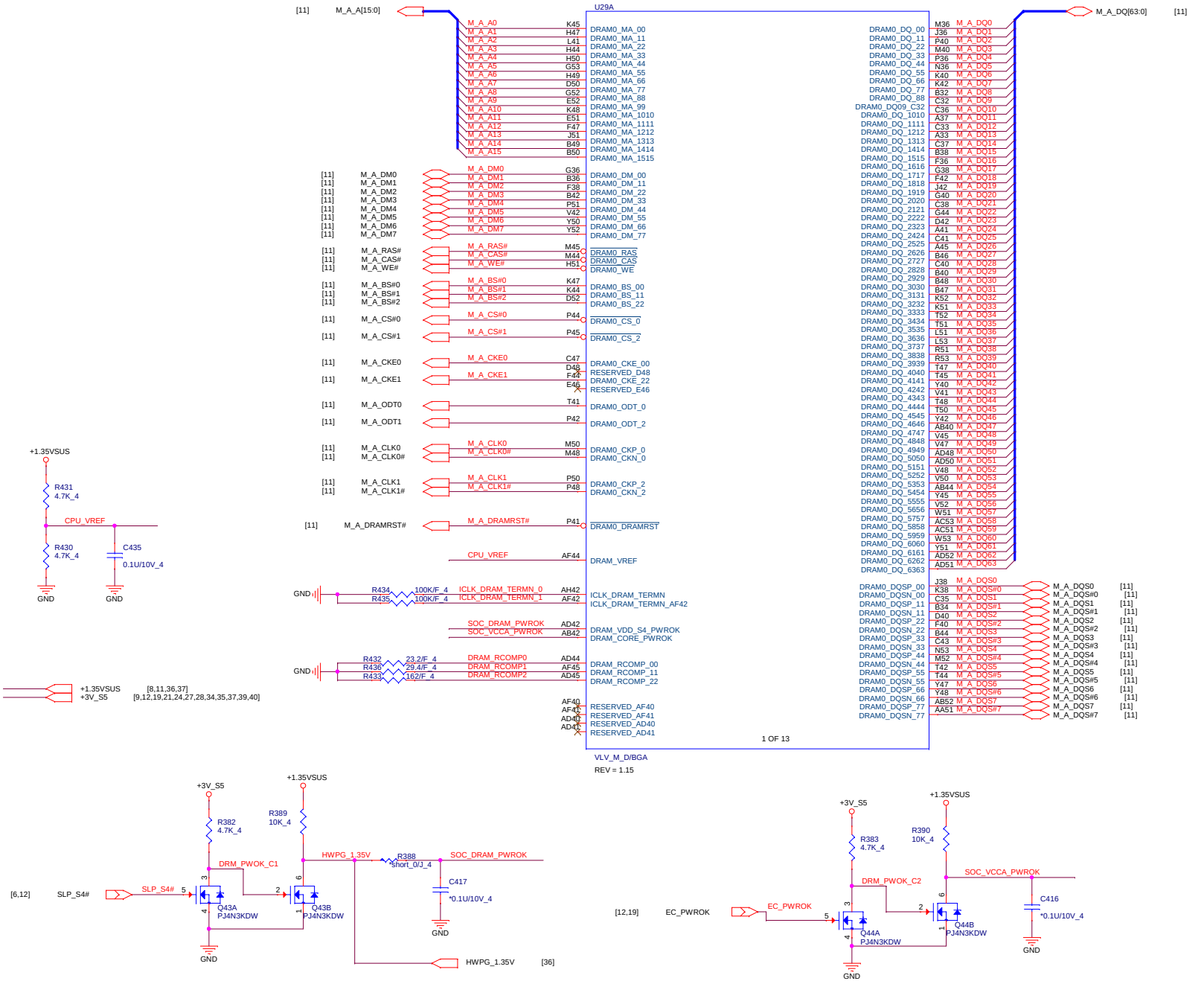
PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SVCC
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SGND
LAYER 6 : BOT



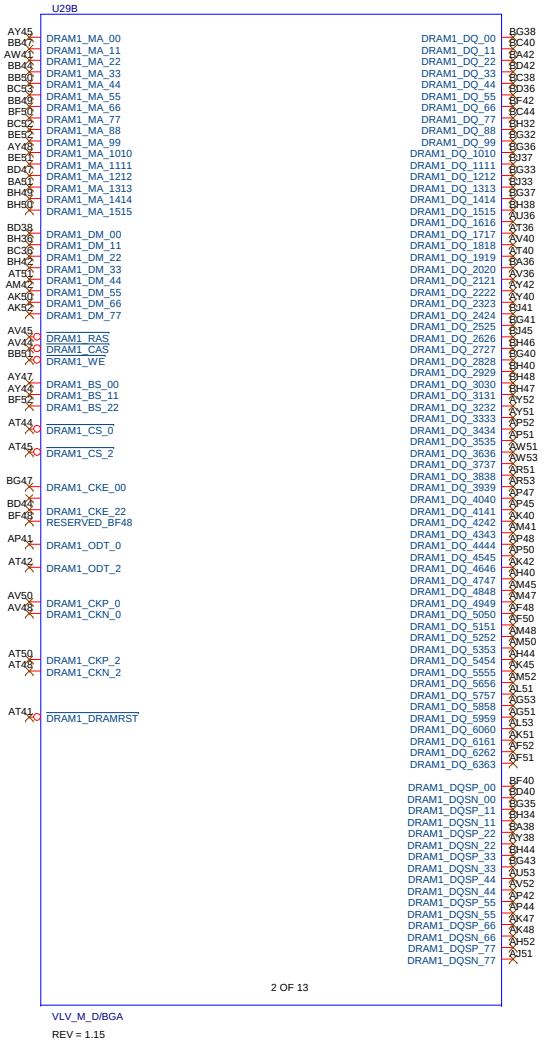
Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	Intel Block Diagram	1A
Date: Thursday, July 10, 2014	Sheet 1 of 44	

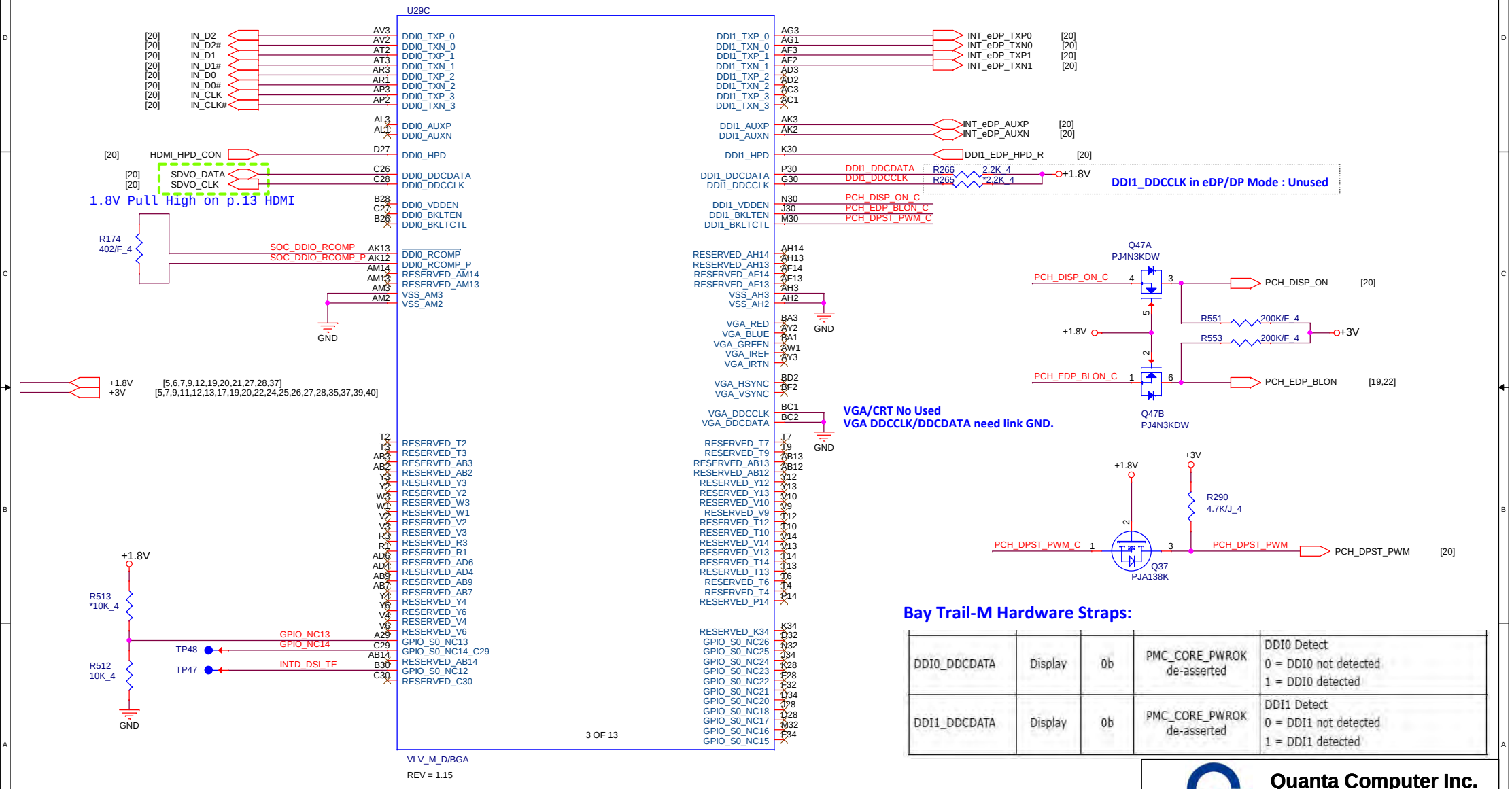


Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	Valley 1/9 (DDRA)	1A
Date: Thursday, July 10, 2014	Sheet 2 of 44	



Quanta Computer Inc.		
PROJECT : ZYL/ZYLA		
Size	Document Number: Valley 2/9 (DDRB)	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 3 of 44	



Bay Trail-M Hardware Straps:

DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	Valley 3/9 (Display)	1A
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SATA HDD

SATA ODD

GPU x2

WLAN x1

LAN x1

201/04/18 : Add GPU Power Control Siganls

201/04/18 : Add GPU Power Control Siganls

Security Flash Descriptors
0 = Override
1 = Normal Operation

0 = LPC
1 = SPI

AC Present: This input pin indicates when the platform is plugged into AC power.

High	UMA Only
Low	GPU power is control by PCH GPIO (Discrete, SG or Optimize)

Default NC No Pull High / Low

Default Pull High 10K(+3V)

Default NC No Pull High / Low

Default Pull Low 10K(GND)

Quanta Computer Inc.	PROJECT : ZYL/ZYLA
Size	Document Number: Valley 4/9 (SD/PCIE/SATA) — Rev: 1A
Date: Thursday, July 10, 2014	Sheet 5 of 44

+1.8V_S5 [7,9,12,21,37]
+1.8V [4,5,7,9,12,19,20,21,27,28,37]

C458 12P/50V_4 — XTAL25_OUT — Y12 25MHZ +-10PPM — R456 1M_4 — XTAL25_IN — C453 12P/50V_4 — GND

U29E

XTAL25_IN AH12 ICLK_OSCIN
XTAL25_OUT AH10 ICLK_OSCOUT
AD9 RESERVED_AD9
R463 4.02K/F_4 ICLK_ICOMP AD14 ICLK_ICOMP
R462 47.5/F_4 ICLK_RCOMP AD13 ICLK_RCOMP
AD10 RESERVED_AD10
AD12 RESERVED_AD12

GPU
[13] CLK_PCIE_VGAN AF6 PCIE_CLKN_00
[13] CLK_PCIE_VGAP AF4 PCIE_CLKP_00
AF9 PCIE_CLKN_11
AF7 PCIE_CLKP_11

WLAN
[28] CLK_PCIE_WLANN AK4 PCIE_CLKN_22
[28] CLK_PCIE_WLANP AK6 PCIE_CLKP_22

LAN
[27] CLK_PCIE_LANN AM4 PCIE_CLKN_33
[27] CLK_PCIE_LANP AM6 PCIE_CLKP_33
AM10 RESERVED_AM10
AM9 RESERVED_AM9

BH7 PMC_PLT_CLK_00
BH6 PMC_PLT_CLK_11
BH4 PMC_PLT_CLK_22
BH5 PMC_PLT_CLK_33
BH3 PMC_PLT_CLK_44
BJ3 PMC_PLT_CLK_55
C15 ILB_RTC_RST

SRT_CRST#
XDP_H_TCK D14 TAP_TCK
XDP_H_TRST# G12 TAP_TRST
XDP_H_TMS F14 TAP_TMS
XDP_H_TDI F12 TAP_TDI
XDP_H_TDO G16 TAP_TDO
XDP_H_PRDY# D18 TAP_PRDY
XDP_H_PREQ# F16 TAP_PREQ
AT34 RESERVED

SOC_SPI_CS# C23 PCU_SPI_CS_00
C21 PCU_SPI_CS_11
SOC_SPI_MISO B22 PCU_SPI_MISO
SOC_SPI_MOSI A21 PCU_SPI_MOSI
SOC_SPI_CLK C22 PCU_SPI_CLK

TP_INT# B18 GPIO_S5_0
SOC_JTAG2_TCK B16 GPIO_S5_1
SOC_JTAG2_TMS C18 GPIO_S5_2
SOC_JTAG2_TDI A17 GPIO_S5_3
SOC_JTAG2_TDO C17 GPIO_S5_4
BOARD_ID4 C16 GPIO_S5_5
BOARD_ID5 B14 GPIO_S5_6
C15 GPIO_S5_7

BOARD_ID1 C13 GPIO_S5_8
BOARD_ID2 A13 GPIO_S5_9
BOARD_ID3 C19 GPIO_S5_10

R529 49.9/F_4 SOC_GPIO_RCOMP N26 GPIO_RCOMP

5 OF 13
VLW_M_D/BGA
REV = 1.15

SIO_UART1_RXD AU34
SIO_UART1_TXD AV34
SIO_UART1_RTS BA34
SIO_UART1_CTS AY34
SIO_UART2_RXD BF34
SIO_UART2_TXD BD34
SIO_UART2_RTS BD32
SIO_UART2_CTS BF32

PMC_SUSPWRDNACK D26 SUS_PWRDOWNACK R264 *short_0_4 SUSWARN#_EC [19]
PMC_SUSCLK0_G24 G24
PMC_SLP_S0IX F18 SLP_S0IX# [12]
PMC_SLP_S4 F22 SLP_S4# [2,12]
PMC_SLP_S3 D22 SLP_S3# [12]
GPIO_S514_J20 J20
PMC_ACPRESENT D20 AC_PRESENT AC_PRESENT [5]
PMC_WAKE_PCIE_0 F26 SOC_PMC_WAKE SOC_PMC_WAKE [12]
PMC_BATLOW K26 PMU_BATLOW#_R
PMC_PWRBTN J26 SOC_PWRBTN# [12]
PMC_RSTBTN BG9 SOC_REST_BTN
PMC_PLTRST F20 SOC_PLTRST# [12]
GPIO_S517_J24 J24
PMC_SUS_STAT G18 PCH_SLP_S0# [12]

ILB_RTC_TEST C11 SOC_RTEST#

PMC_RSMRST B10 SOC_RSMRST# [12]
PMC_CORE_PWROK B7 CORE_PWROK [12]

ILB_RTC_X1 C9 RTC_X1
ILB_RTC_X2 A9 RTC_X2
ILB_RTC_EXTPAD B8 BRTC_EXTPAD C482 0.1U/10V_4 GND

SVID_ALERT B24 SVID_ALERT#_SOC R517 20/F_4 VR_SVID_ALERT# VR_SVID_ALERT# [35]
SVID_DATA A25 SVID_DATA_SOC R518 16.9R_4 VR_SVID_DATA VR_SVID_DATA [35]
SVID_CLK C25 SVID_CLK_SOC R519 *0/short_4 VR_SVID_CLK VR_SVID_CLK [35]

SIO_PWM_00 AU32 TOUCHPANEL_INTR#_SOC R90 *10K_4 +1.8V
SIO_PWM_11 AT32 SOC_SENS_HUB_RST# R96 *10K_4

GPIO_S5_22 K24
GPIO_S5_23 N24
GPIO_S5_24 N20
GPIO_S5_25 J18
GPIO_S5_26 M18
GPIO_S5_27 K18
GPIO_S5_28 K20
GPIO_S5_29 M22
GPIO_S5_30 N24

SIO_SPI_CS AV32
SIO_SPI_MISO BA28
SIO_SPI_MOSI AY28
SIO_SPI_CLK AY30

+1.8V_S5
R248 51/F_4 XDP_H_TDO
R260 51/F_4 XDP_H_TMS
R228 51/F_4 XDP_H_TDI
R247 200/F_4 XDP_H_PREQ#
R229 51/F_4 XDP_H_TRST#
R246 51/F_4 XDP_H_TCK
GND

TP28

Touch pad [21] TP_INT#
+1.8V_S5
R505 10K_4 TP_INT#
R493 *10K_4 SOC_JTAG2_TCK
R494 *10K_4 SOC_JTAG2_TMS
R514 *10K_4 SOC_JTAG2_TDI
R504 *10K_4 SOC_JTAG2_TDO
[12] SOC_KCB_SMI R492 *short_0/J_4 SOC_GPOI7

+1.8V_S5
PMU_BATLOW#_R R242 10K_4
SUS_PWRDOWNACK R263 10K_4
SOC_PMC_WAKE R243 10K_4
AC_PRESENT R262 10K_4
+1.8V
SOC_REST_BTN R409 10K_4

+1.0V
C293 *0.1u/10V_4 GND
R526 *71.5/F_4
R525 71.5/F_4
R527 *71.5/F_4
VR_SVID_DATA
VR_SVID_ALERT#
VR_SVID_CLK

intel check list 2.0: 70 Ω ±5% pull-up to V1P0S,
PLM does not have it, so use 71.5 Ω ±1% to replace.

RTC Clock 32.768KHz

RTC_X1 — 15P/50V_4 C477 — Y13 32.768KHZ — R487 10M_4 — 15P/50V_4 C476 — RTC_X2 — GND

2013/07/25
change package , P/N change
from B6332768224 to
B6332768453

SPI NOR FLASH

+1.8V_S5
C513 0.1U/10V_4 GND
U33
VCC SPI_SI
SPI_SO
CS#
WP# SPI_SCK
SPI_HOLD GND
SPI_FLASH
soic8-7_9-1_27
AKE5EZN0N00
IC FLASH (8P) W25Q64FWSSIG (SOIC)
R561 3.3K/F_4 SPI_3P
R557 3.3K/F_4 SPI_7P
GND

SOC_SPI_MOSI_R → R563 *short_0/J_4 → SOC_SPI_MOSI
SOC_SPI_MISO_R → R558 *short_0/J_4 → SOC_SPI_MISO
SOC_SPI_CS#_R → R554 *short_0/J_4 → SOC_SPI_CS#
SOC_SPI_CLK_R → R560 *short_0/J_4 → SOC_SPI_CLK

R556 EC18@0/J_4
R555 EC18@0/J_4
R559 EC18@0/J_4
R564 EC18@0/J_4
SOC_SPI_CLK_R1 [19]
SOC_SPI_CS#_R1 [19]
SOC_SPI_MISO_R1 [19]
SOC_SPI_MOSI_R1 [19]

+1.8V_S5
R552 3.3K/F_4 SOC_SPI_CS#

BOARD ID

+1.8V_S5
R502 UMA@10K_4 BOARD_ID1 R490 EV@10K_4
R503 *10K_4 BOARD_ID2 R491 10K_4
R506 *TPM@10K_4 BOARD_ID3 R495 10K_4
R537 *10K_4 BOARD_ID4 R543 10K_4
R535 *10K_4 BOARD_ID5 R534 10K_4

BOARD_ID1 : UMA or DIS HIGH= UMA, LOW= DIS
BOARD_ID2 : None
BOARD_ID3 : TPM HIGH=TPM, LOW=W/O TPM
BOARD_ID4 : Reserve for UMA and GPU
BOARD_ID5 : Reserve for UMA and GPU

RTC Circuitry(RTC)

+3V_RTC_0
20mils
+3VPCU
+3V_RTC_0 R520 1K/J_4 VCCRTC_1
20MIL
D32 BAT54C
CN17 BAT_CONN
GND
20MIL

+3V_RTC
R542 20K/J_4
30mils
R536 20K/J_4
C503 1u/6.3V_4
C504 1u/6.3V_4
C498 1u/6.3V_4
G10 *SHORT_PAD1
G9 *SHORT_PAD1
SOC_RTEST#
SRT_CRST#
20MIL

6/25 Change G9、G10 footprint from "SOLDERJUMPER-2" to "RC0603-C" for SMT request

Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	Valley 5/9 (SPI/GPIO/CLK)	1A
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+1.8V_S5 [6,9,12,21,37]
+1.8V [4,5,6,9,12,19,20,21,27,28,37]
+3V [4,5,9,11,12,13,17,19,20,22,24,25,26,27,28,35,37,39,40]

U29F

Port 1 is debug port

USB3.0

USB 2.0 HUB

Bluetooth

CAMERA

GPIO_S5_31 GPIO_S5_32 GPIO_S5_33 GPIO_S5_34 GPIO_S5_35 GPIO_S5_36 GPIO_S5_37 GPIO_S5_38 GPIO_S5_39 GPIO_S5_40 GPIO_S5_41 GPIO_S5_42 GPIO_S5_43

R475 *10K_4 SOC_PWR_BUT

USBP0+ USBP0- USB_H1_P USB_H1_N USBP2+ USBP2- USBP3+ USBP3-

USB_DP0 USB_DN0 USB_DP1 USB_DN1 USB_DP2 USB_DN2 USB_DP3 USB_DN3

R244 1K_4 ICLK_USB_TERMN_0
R245 1K_4 ICLK_USB_TERMN_1
ICLK_USB_TERMN_D10 ICLK_USB_TERMN

SOC_USB_OC0 SOC_USB_OC1
R515 10K_4 R516 10K_4
USB_OC_00 USB_OC_11

R219 45.3/F_4 USB_RCOMP
USB_RCOMPO USB_RCOMPI

R478 *0/J_4 USB_PLL_MON
USB_PLL_MON

USB_HSIC0_DATA USB_HSIC0_STROBE

USB_HSIC1_DATA USB_HSIC1_STROBE

R489 45.3/F_4 USB_HSIC_RCOMP
R124 49.9/F_4
USB_HSIC_RCOMP

LPC_RCOMP

LAD0 LAD1 LAD2 LAD3 LFRAME# CLK_24M_KBC CLK_24M_DEBUG CLKRUN# SOC_SERIRQ SOC_CLKOUT_0 SOC_CLKOUT_1 SOC_CLKRUN# SOC_SERIRQ

R428 22_4 R411 *22_4 For TPM
R427 *22_4 R429 22_4

ILB_LPC_AD_00 ILB_LPC_AD_11 ILB_LPC_AD_22 ILB_LPC_AD_33 ILB_LPC_FRAME ILB_LPC_CLK_00 ILB_LPC_CLK_11 ILB_LPC_CLKRUN ILB_LPC_SERIRQ

R394 2.2K_4 R410 2.2K_4 R426 2.2K_4
SMB_SOC_DATA SMB_SOC_CLK SMB_SOC_ALERTB
PCU_SMB_DATA PCU_SMB_CLK PCU_SMB_ALERT

Q46 PJ4N3KDW
SMB_SOC_DATA SMB_SOC_CLK
4.7K_4 R392 4.7K_4 R387
SMB_RUN_DAT SMB_RUN_CLK

6 OF 13

VLV_M_D/BGA
REV = 1.15

RESERVED_M10 RESERVED_M9 RESERVED_P7 RESERVED_P6 RESERVED_M7 USB3_REXT0 RESERVED_P10 RESERVED_P12 RESERVED_M4 RESERVED_M6 USB3_RXP0 USB3_RXN0 USB3_TXP0 USB3_TXN0 RESERVED_H8 RESERVED_H7 RESERVED_H5 RESERVED_H4

USB3_P0_REXT R477 1.24K/F_4

USB30_RX1+ USB30_RX1- USB30_TX1+ USB30_TX1-

Top Swap (A16 Override)
0 = Top address bit is unchanged
1 = Top address bit is inverted

R120 *10K_4 R113 *10K_4

GPIO_S0_SC_55 GPIO_S0_SC_56 GPIO_S0_SC_57 GPIO_S0_SC_58 GPIO_S0_SC_59 GPIO_S0_SC_60 GPIO_S0_SC_61
GPIO_S0_SC_56 SOC_UART_TX SOC_UART_RX

ILB_8254_SPKR SPKR

SIO_I2C0_DATA SIO_I2C0_CLK I2C_0_SDA_R I2C_0_SCL_R R420 22/J_4 R421 22/J_4 I2C_0_SDA I2C_0_SCL
Touch pad

SIO_I2C1_DATA SIO_I2C1_CLK I2C_1_SDA I2C_1_SCL

SIO_I2C2_DATA SIO_I2C2_CLK I2C_2_SDA_R I2C_2_SCL_R

SIO_I2C3_DATA SIO_I2C3_CLK I2C_3_SDA I2C_3_SCL

SIO_I2C4_DATA SIO_I2C4_CLK I2C_4_SDA I2C_4_SCL

SIO_I2C5_DATA SIO_I2C5_CLK I2C_5_SDA I2C_5_SCL

SIO_I2C6_DATA SIO_I2C6_CLK I2C_6_SDA I2C_6_SCL

GPIO_S0_SC_092 GPIO_S0_SC_093 I2C_NFC_SOC_SDA I2C_NFC_SOC_SCL T10 T9

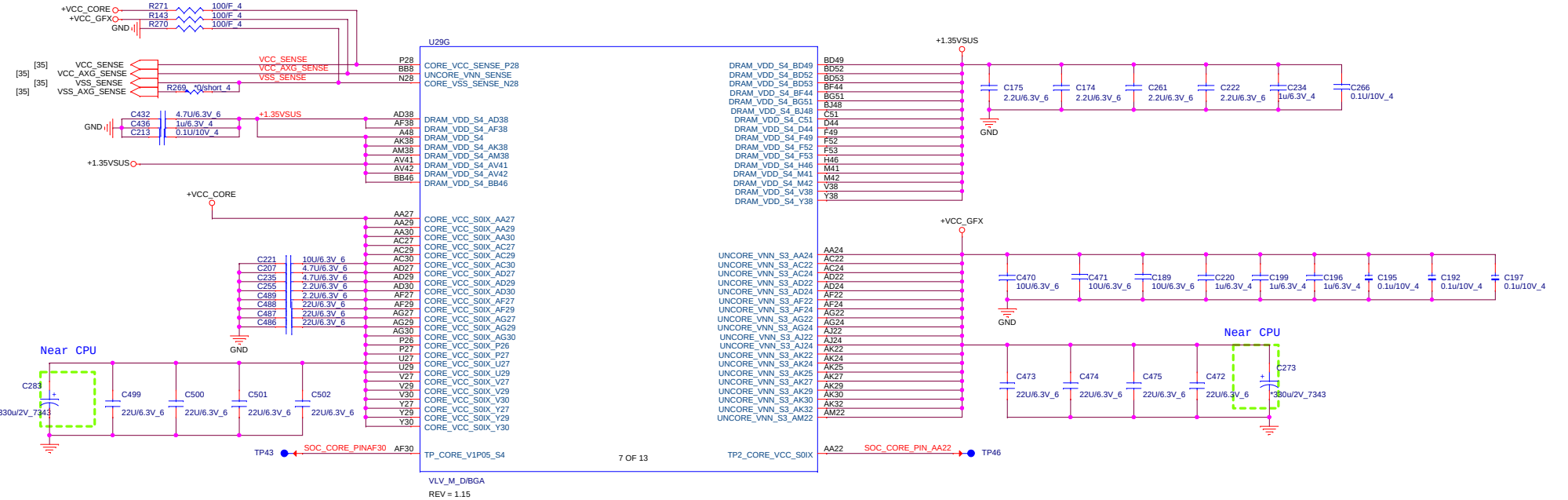
SOC_UART_TX R126 *0/J_4 SOC_UART_RX
Un-Stuff for Test Only

I2C_0_SDA R403 560_4 I2C_0_SCL R404 560_4
I2C_1_SDA R422 *560_4 I2C_1_SCL R405 *560_4
I2C_2_SDA_R R423 *560_4 I2C_2_SCL_R R399 *560_4
I2C_3_SDA R395 *560_4 I2C_3_SCL R416 *560_4
I2C_4_SDA R406 *560_4 I2C_4_SCL R396 *560_4
I2C_5_SDA R417 *560_4 I2C_5_SCL R400 *560_4
I2C_6_SDA R397 *560_4 I2C_6_SCL R407 *560_4
I2C_NFC_SOC_SDA R424 *560_4 I2C_NFC_SOC_SCL R425 *560_4

I2C pull up:
Standard/ Fast Mode --> 560 ohm
Hight speed mode --> CLK- 560 ohm;
DATA- 910 ohm

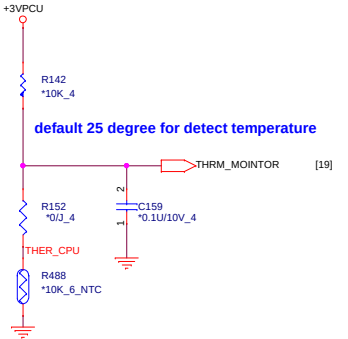
Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	Valley 6/9 (USB/LPC/I2C)	1A
Date: Thursday, July 10, 2014	Sheet 7 of 44	



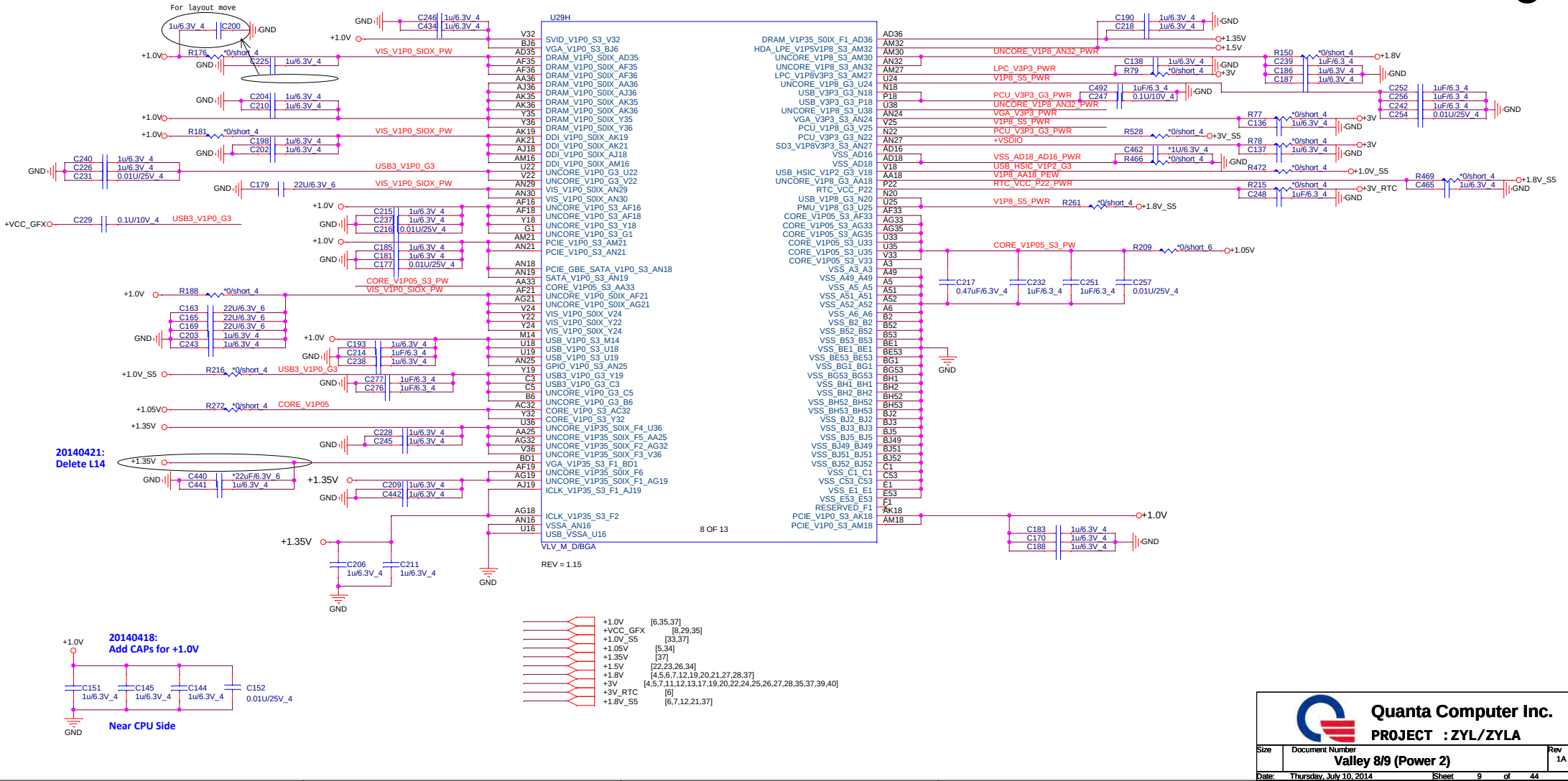
+VCC_CORE [29,35]
+VCC_GFX [9,29,35]
+1.35VSUS [2,11,36,37]
+3VPCU [6,19,21,22,25,26,30,31,32,37,39,40]

IO Thrm Protect



Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	Valley 7/9 (Power 1)	1A
Date: Thursday, July 10, 2014	Sheet 8 of 44	


For layout move
U29H
SVID_V1P0_S3_V32
VGA_V1P0_S3_BJ6
DRAM_V1P0_S0IX_AD35
DRAM_V1P0_S0IX_AF35
DRAM_V1P0_S0IX_AF36
DRAM_V1P0_S0IX_AA36
DRAM_V1P0_S0IX_AJ36
DRAM_V1P0_S0IX_AK35
DRAM_V1P0_S0IX_AK36
DRAM_V1P0_S0IX_Y35
DRAM_V1P0_S0IX_Y36
DDI_V1P0_S0IX_AK19
DDI_V1P0_S0IX_AK21
DDI_V1P0_S0IX_AJ18
DDI_V1P0_S0IX_AM16
UNCORE_V1P0_G3_U22
UNCORE_V1P0_G3_V22
VIS_V1P0_S0IX_AN29
VIS_V1P0_S0IX_AN30
UNCORE_V1P0_S3_AF16
UNCORE_V1P0_S3_AF18
UNCORE_V1P0_S3_Y18
UNCORE_V1P0_S3_G1
PCIE_V1P0_S3_AM21
PCIE_V1P0_S3_AN21
PCIE_GBE_SATA_V1P0_S3_AN18
SATA_V1P0_S3_AN19
CORE_V1P05_S3_AA33
UNCORE_V1P0_S0IX_AF21
UNCORE_V1P0_S0IX_AG21
VIS_V1P0_S0IX_V24
VIS_V1P0_S0IX_Y22
VIS_V1P0_S0IX_Y24
USB_V1P0_S3_M14
USB_V1P0_S3_U18
USB_V1P0_S3_U19
GPIO_V1P0_S3_AN25
USB3_V1P0_G3_Y19
USB3_V1P0_G3_C3
UNCORE_V1P0_G3_C5
UNCORE_V1P0_G3_B6
CORE_V1P0_S3_AC32
CORE_V1P0_S3_Y32
UNCORE_V1P35_S0IX_F4_U36
UNCORE_V1P35_S0IX_F5_AA25
UNCORE_V1P35_S0IX_F2_AG32
UNCORE_V1P35_S0IX_F3_V36
VGA_V1P35_S3_F1_BD1
UNCORE_V1P35_S0IX_F6
UNCORE_V1P35_S0IX_F1_AG19
ICLK_V1P35_S3_F1_AJ19
ICLK_V1P35_S3_F2
VSSA_AN16
USB_VSSA_U16
VLV_M_D/BGA
8 OF 13
REV = 1.15
DRAM_V1P35_S0IX_F1_AD36
HDA_LPE_V1P5V1P8_S3_AM32
UNCORE_V1P8_S3_AM30
UNCORE_V1P8_S3_AN32
LPC_V1P8V3P3_S3_AM27
UNCORE_V1P8_G3_U24
USB_V3P3_G3_N18
USB_V3P3_G3_P18
UNCORE_V1P8_S3_U38
VGA_V3P3_G3_N24
PCU_V1P8_G3_V25
PCU_V3P3_G3_N22
SD3_V1P8V3P3_S3_AN27
VSS_AD16
VSS_AD18
USB_HSIC_V1P2_G3_V18
UNCORE_V1P8_G3_AA18
RTC_VCC_P22
USB_V1P8_G3_N20
PMU_V1P8_G3_U25
CORE_V1P05_S3_AF33
CORE_V1P05_S3_AG33
CORE_V1P05_S3_AG35
CORE_V1P05_S3_U33
CORE_V1P05_S3_U35
CORE_V1P05_S3_V33
VSS_A3_A3
VSS_A49_A49
VSS_A5_A5
VSS_A51_A51
VSS_A52_A52
VSS_A6_A6
VSS_B2_B2
VSS_B52_B52
VSS_B53_B53
VSS_BE1_BE1
VSS_BE53_BE53
VSS_BG1_BG1
VSS_BG53_BG53
VSS_BH1_BH1
VSS_BH2_BH2
VSS_BH52_BH52
VSS_BH53_BH53
VSS_BJ2_BJ2
VSS_BJ3_BJ3
VSS_BJ5_BJ5
VSS_BJ49_BJ49
VSS_BJ51_BJ51
VSS_BJ52_BJ52
VSS_C1_C1
VSS_C53_C53
VSS_E1_E1
VSS_E53_E53
RESERVED_F1
PCIE_V1P0_S3_AK18
PCIE_V1P0_S3_AM18
UNCORE_V1P8_AN32_PWR
LPC_V3P3_PWR
V1P8_S5_PWR
PCU_V3P3_G3_PWR
VGA_V3P3_PWR
+VSDIO
VSS_AD18_AD16_PWR
USB_HSIC_V1P2_G3
V1P8_AA18_PEW
RTC_VCC_P22_PWR
CORE_V1P05_S3_PW
VIS_V1P0_SIOX_PW
USB3_V1P0_G3
20140421:
Delete L14
20140418:
Add CAPs for +1.0V
Near CPU Side
+1.0V [6,35,37]
+VCC_GFX [8,29,35]
+1.0V_S5 [33,37]
+1.05V [5,34]
+1.35V [37]
+1.5V [22,23,26,34]
+1.8V [4,5,6,7,12,19,20,21,27,28,37]
+3V [4,5,7,11,12,13,17,19,20,22,24,25,26,27,28,35,37,39,40]
+3V_RTC [6]
+1.8V_S5 [6,7,12,21,37]
Quanta Computer Inc.
PROJECT : ZYL/ZYLA
Size
Document Number
Valley 8/9 (Power 2)
Rev
1A
Date: Thursday, July 10, 2014
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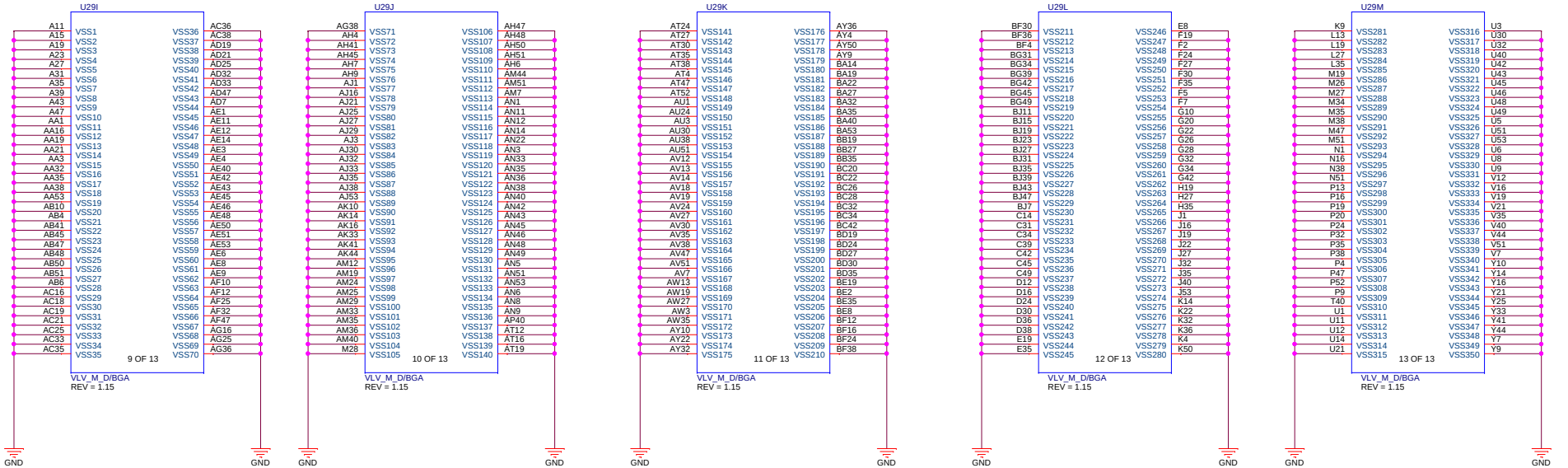

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PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	Valley 9/9 (GND)	1A
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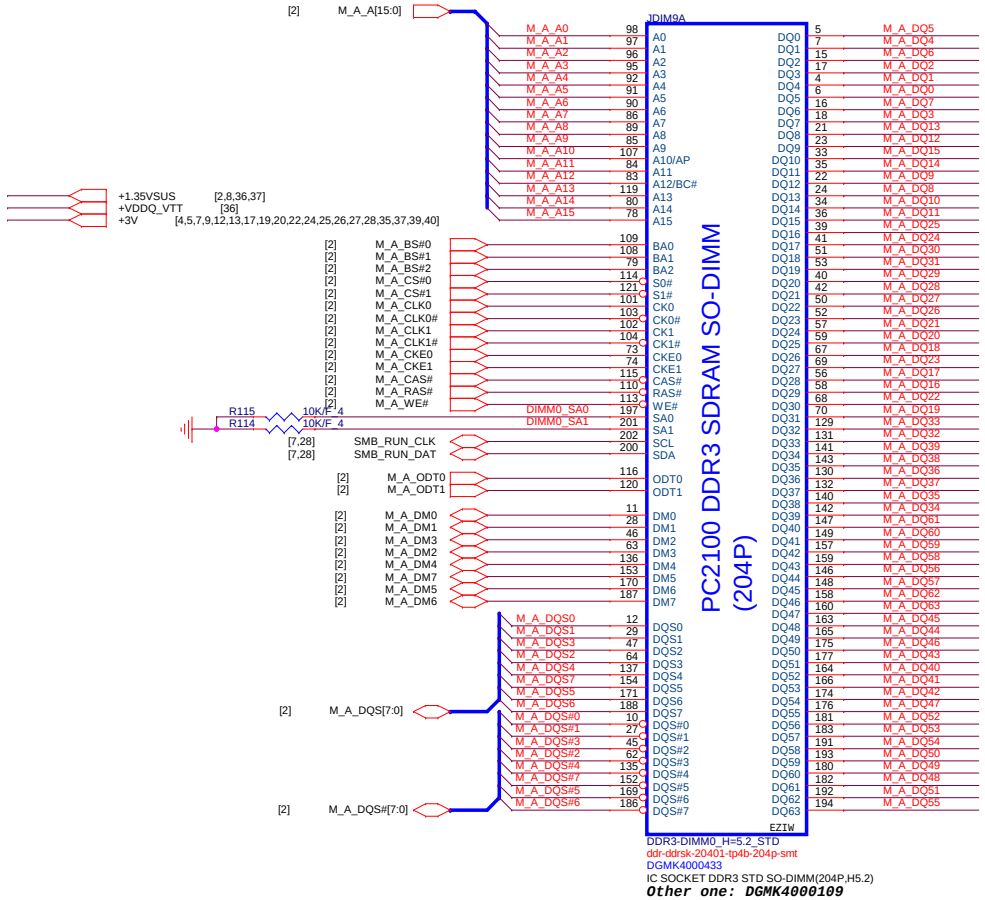
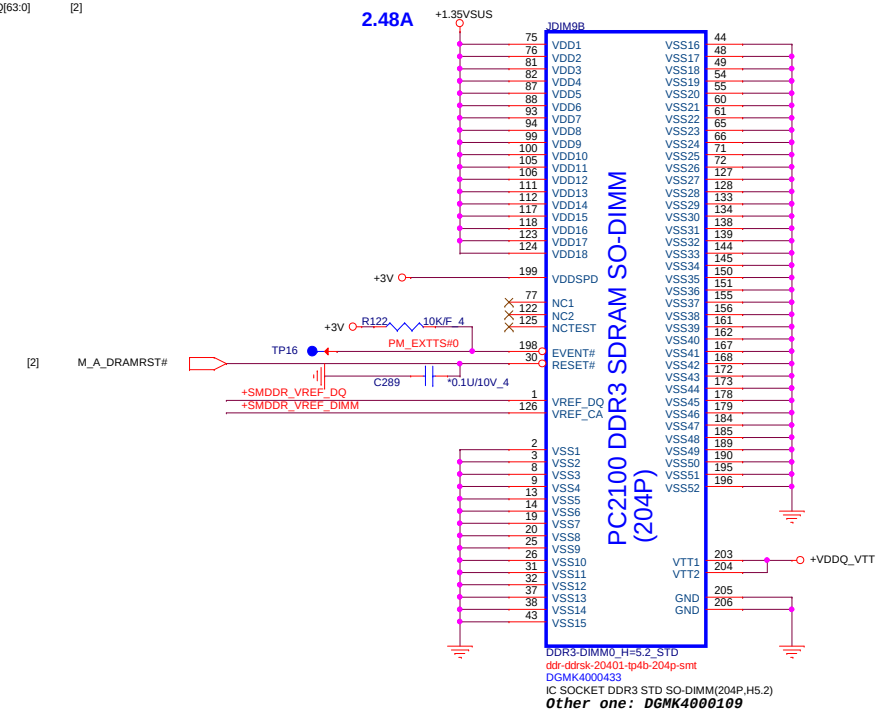
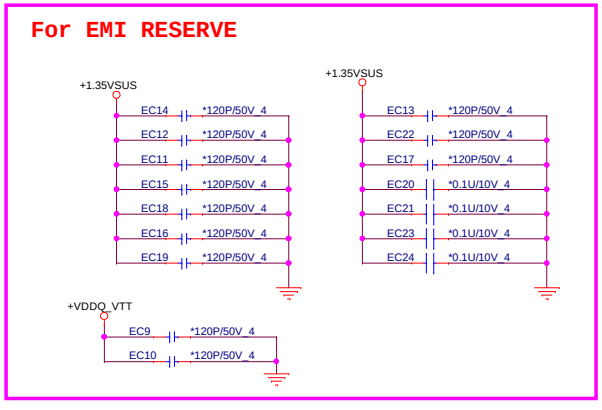
Address A0H



2.48A

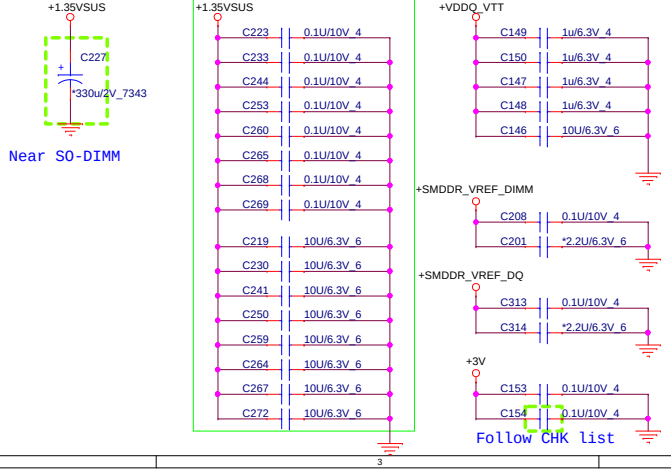


For EMI RESERVE

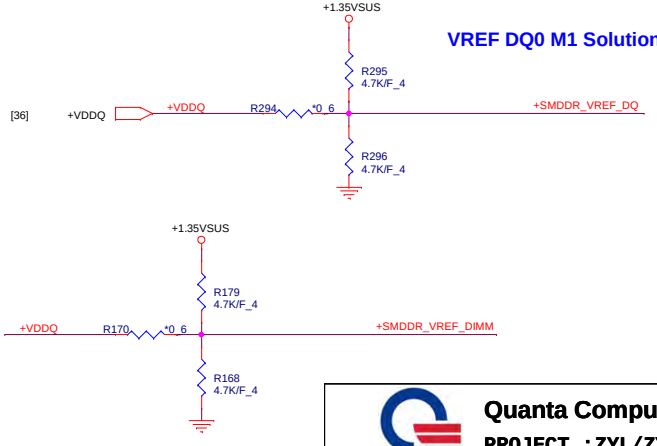


Place these Caps near So-Dimm0.

0.1uF/10uF 4pcs on each side of connector



VREF DQ0 M1 Solution



Quanta Computer Inc.			
PROJECT : ZYL/ZYLA			
Size	Document Number		Rev
	DDR3 DIMM0-STD(5.2H)		1A
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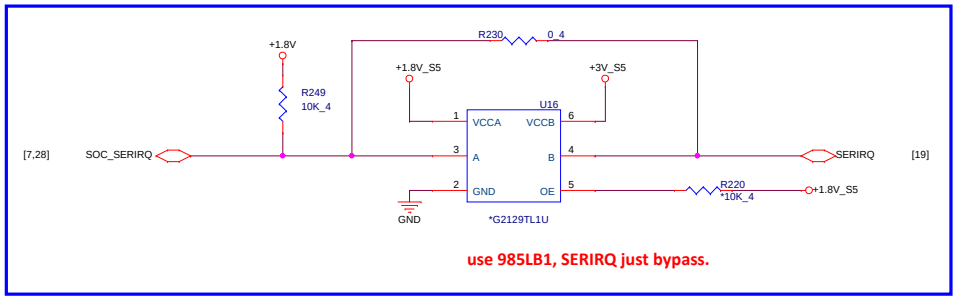

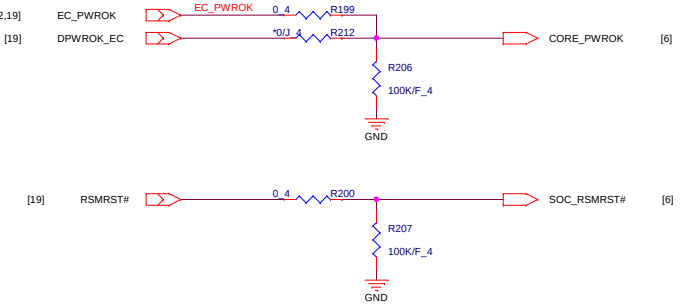

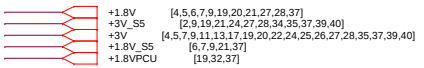

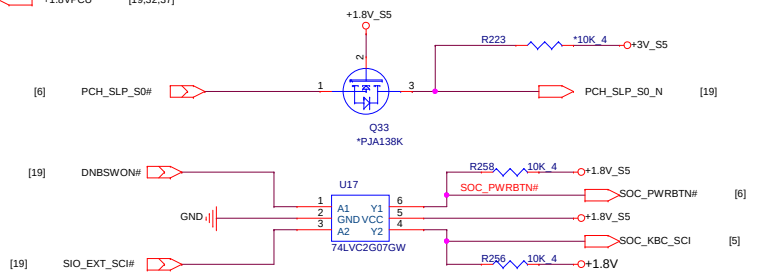

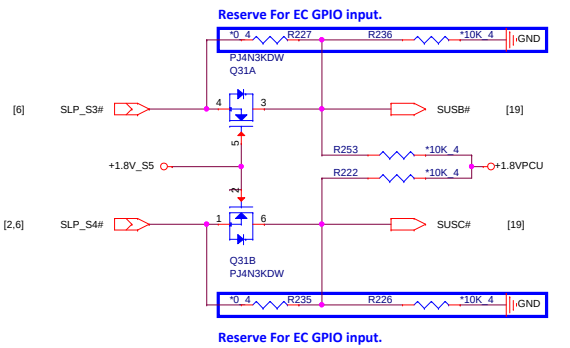

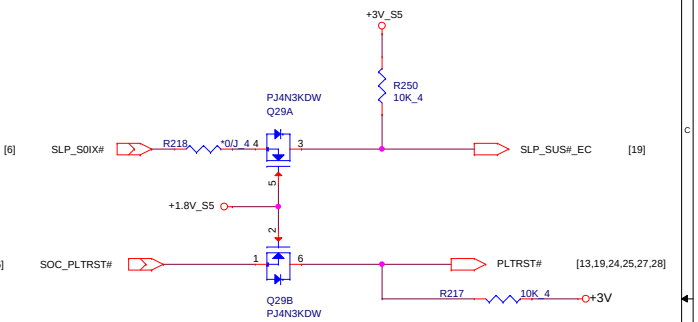

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PROJECT : ZYL/ZYLA

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<VGA>

1000mA

2500mA

210mA of +3V_GFX

PLACE UNDER GPU BALLS

PLACE NEAR GPU

4.7uF x 15 population x10

0.1uF x 8 population x 4

not GC6 2.0 unstuff resistor

for meet Power down sequence for +3V_GFX

No stuff D8 when GC6 support.

8mils width (0.2MM)

PEX_PLLVDD : 0.3MM = 12mils (150mA)
RSVD R1 and C1 for GV2 co-layout sDDR3 R1

Follow Z09 to isolate CLK_REQ#

PU at page 9

0.4MM = 16mils

0.4MM = 16mils

47u x1 22u x7 stuff x 1 4.7u x6 stuff x 5 330u x1 RSVD by DG

0817 RSVD more NVVDD caps by NV DG

N15x Power on sequance

PEX_RST timing

PCH control PEGX_RST#

Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T_{PVPERL_G}	$T_{PVPERL\_G} \geq 1us$	
$T_{PERST\_CLK\_G}$	$T_{PERST\_CLK\_G} \geq 1T_{REF\_CLK}$	

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Size	Document Number	Rev
	DGPU 1/5 (PEG)	1A

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<VGA>

N15V-GM no support GC6 function.

For Fermi

C87 close ball H22 35mA

PLACE CLOSE TO GPU BALLS

PLACE CLOSE TO BGA

sDDR3
R47=42.2/F
R50=51.1/F

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Size	Document Number	Rev
	DGPU 2/5 (Memory)	1A
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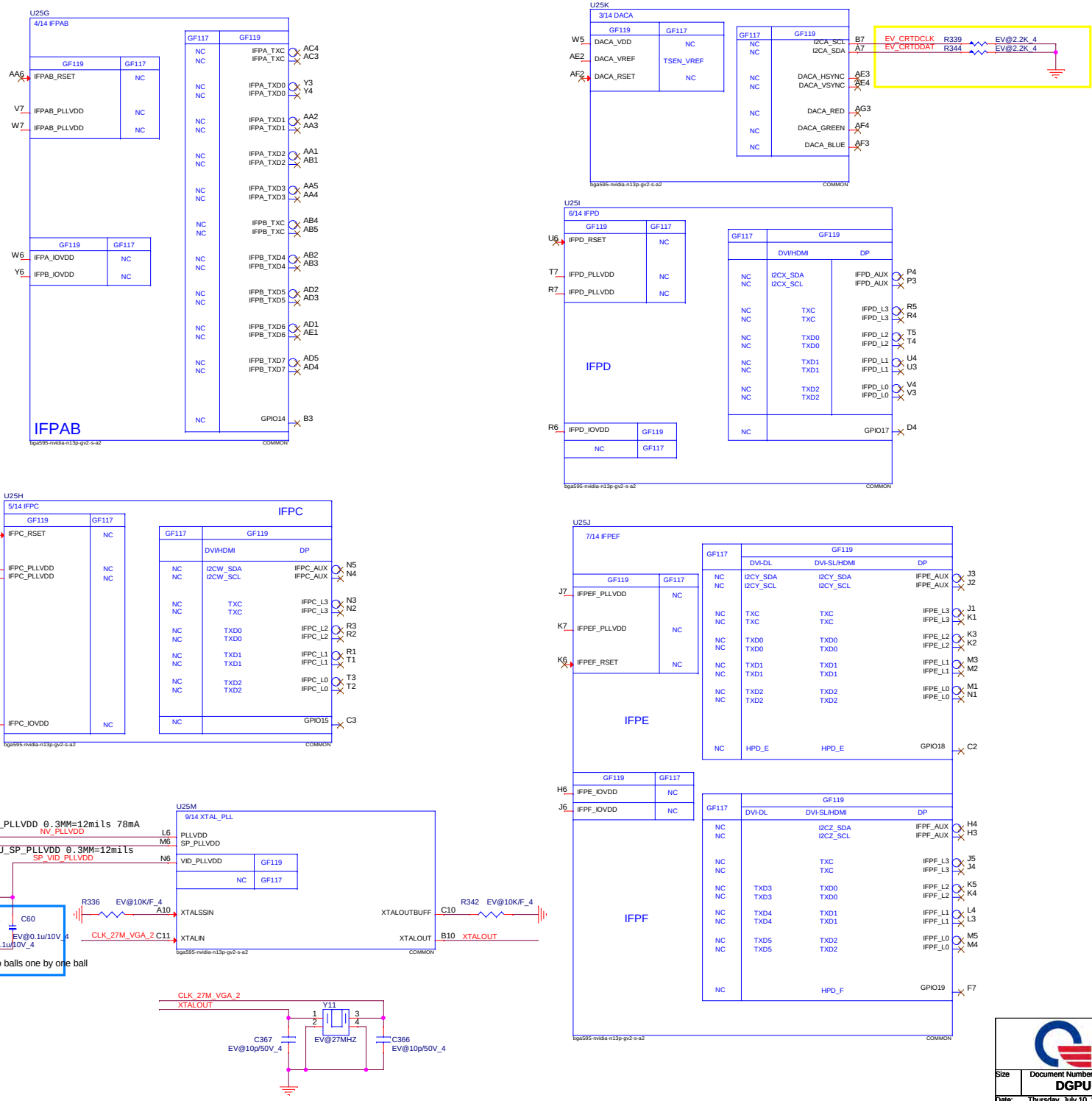
U25G
4/14 IFPAB
IFPAB
U25K
3/14 DACA
U25I
6/14 IFPD
IFPD
U25H
5/14 IFPC
IFPC
U25J
7/14 IFPEF
IFPE
IFPF
U25M
9/14 XTAL_PLL
NV_PLLVDD 0.3MM=12mils 78mA
GPU_SP_PLLVDD 0.3MM=12mils
close to balls one by one ball
Near GPU
Under GPU
EV_CRTDCLK
EV_CRTDDAT
Y11
EV@27MHZ
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PROJECT : ZYL/ZYLA
DGPU 3/5 (Display)
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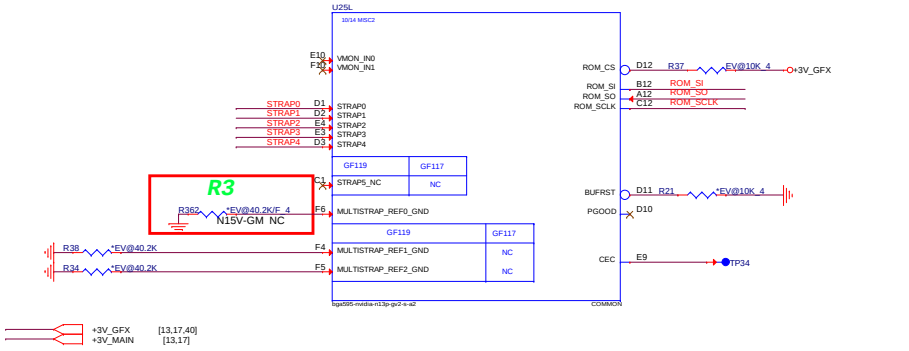
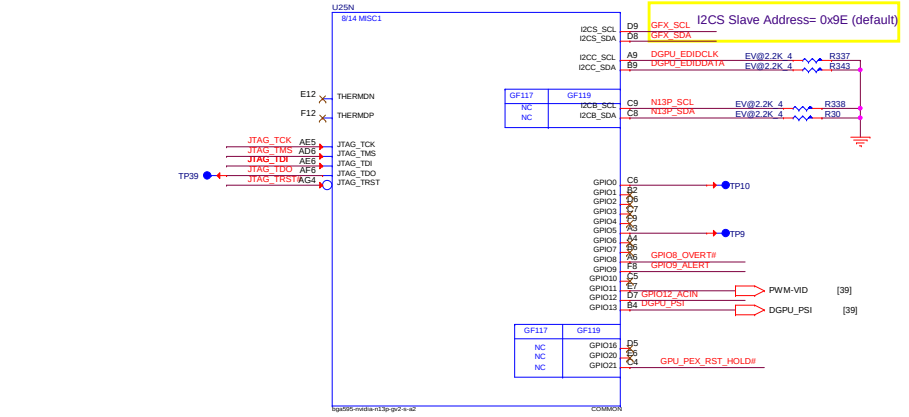
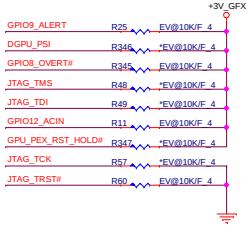
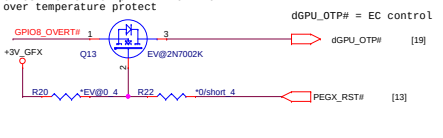
<VGA>

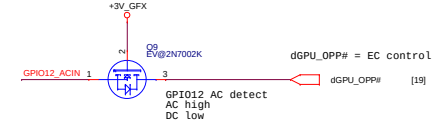






GPIO8 VGA thrmtrip# => inform EC over temperature protect

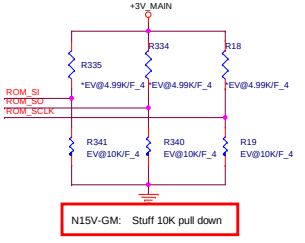


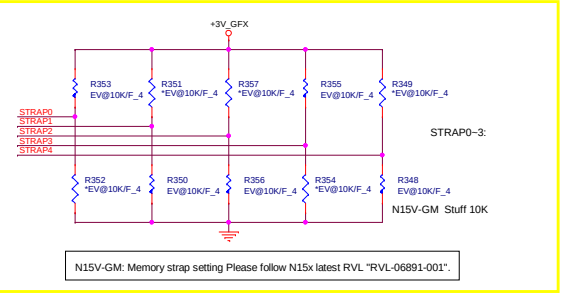


GPIO12 AC detect
AC high
DC low

Binary mode strapping:
For N15V-GM-B sku:
Device ID=0x1140
R3= N.C.
1.ROM_SCLK =10K pull down.
2.ROM_SI= 10k pull down
3.ROM_SO= 10k pull down
4.Strap3~0 = RVL memory binary mode setting.
5.Strap4 =10k pull down

Vendor	Vendor P/N	Strap0	Strap1	Strap2	Strap3	
HYNIX	HT5C4G63AFR-11C	0	0	1	0	
MICRON	MT41J256M16HA-093G:E	1	0	1	1	
SAMSUNG	K4W4G164D-BC1A	1	0	0	1	Default





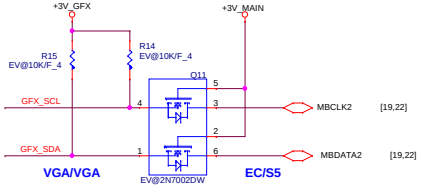
N15V-GM VRAM Configuration Table:

	Strap [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N
4Gb	0100 (0x4) 1101 (0xD) 1001 (0x9)	DDR3 256MBx16,1000MHz DDR3 256MBx16,1000MHz DDR3 256MBx16,1000MHz	HYNIX MICRON SAMSUNG	H5TC4G63AFR-11C MT41J256M16HA-093G:E K4W4G1646D-BC1A	

STRAP3
Optimus ---> 4.99k PD

Resistor P/N
10K ---> CS31002FB26

SMBus(VGA)



Vendor P/N	820M		QCI P/N
N15V-GM-B-A2	GeForce 820M	0x1140	AJ0N15V0T03

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Size	Document Number	Rev
	DGPU 4/5 (MIO/GPIO)	1A

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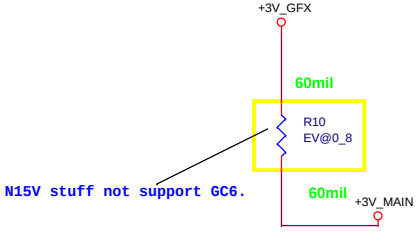
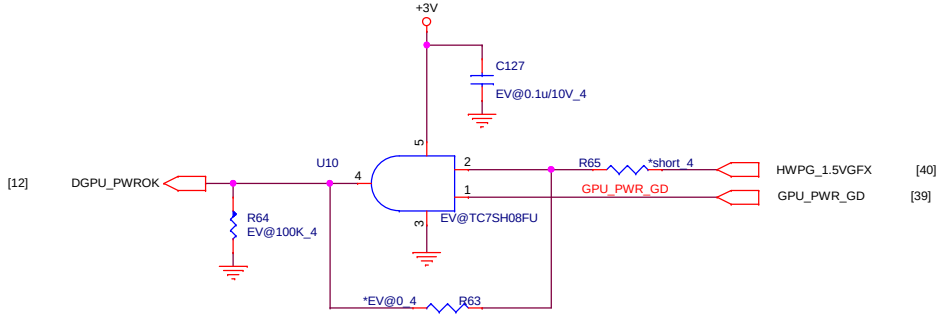
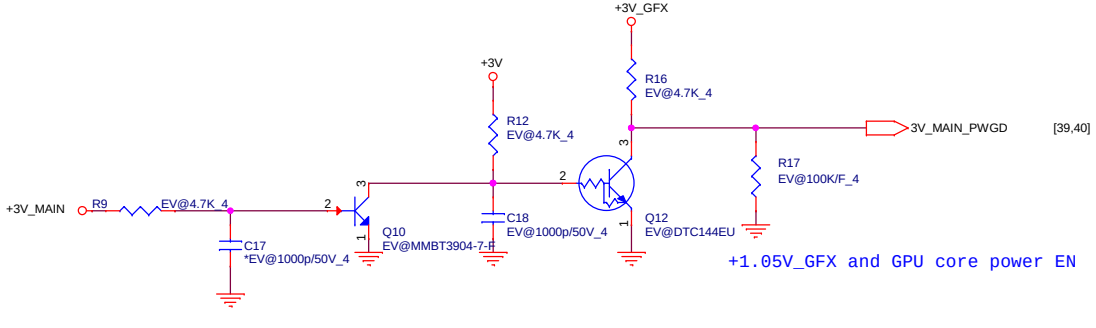
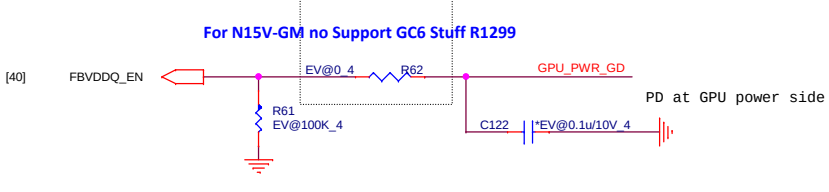
+3V_GFX [13,16,40]
+3V_MAIN [13,16]
+3V [4,5,7,9,11,12,13,19,20,22,24,25,26,27,28,35,37,39,40]









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Size	Document Number	Rev
	DGPU 5/5 (Power/Ground)	1A
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CHANNEL A: 2048MB DDR3X16

+1.05V_GFX [13,14,15,40]

[14] VMA_DQ[63..0]
[14] VMA_DM[7..0]
[14] VMA_WDQS[7..0]
[14] VMA_RDQS[7..0]

VRAM9 / VRAM11 / VRAM10 / VRAM12

96-BALL SDRAM DDR3

EV@VRAM _DDR3_HYNIX_256MX16

Should be 240 Ohms +-1%

R33 EV@243/F_4 (VRAM9)
R358 EV@243/F_4 (VRAM11)
R50 EV@243/F_4 (VRAM10)
R365 EV@243/F_4 (VRAM12)

+1.5V_GFX

[14] FBA_CMD17 → TP11
[14] FBA_CMD1 → TP35
10/14 modify

R31 EV@162/F_4 (VMA_CLK0 / VMA_CLK0#)

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R360 EV@1.33K/F_4, C372 EV@0.1u/10V_4, R361 EV@1.33K/F_4 (VREFC_VMA1)
R23 EV@1.33K/F_4, C26 EV@0.1u/10V_4, R26 EV@1.33K/F_4 (VREFD_VMA1)

R58 EV@162/F_4 (VMA_CLK1 / VMA_CLK1#)

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R47 EV@1.33K/F_4, C96 EV@0.1u/10V_4, R44 EV@1.33K/F_4 (VREFC_VMA3)
R371 EV@1.33K/F_4, C386 EV@0.1u/10V_4, R370 EV@1.33K/F_4 (VREFD_VMA3)

C132 C393 C121 C384 EV@1u/10V_4
C34 C404 C371 C381 C365 C23 EV@10u/6.3V_6 / EV@1u/10V_4
C362 C364 C390 C124 EV@10u/6.3V_6 / EV@1u/10V_4
C37 C113 C24 C368 EV@1u/10V_4
C400 C128 EV@10u/6.3V_6
C363 C370 C403 EV@0.1u/10V_4
C369 C114 EV@0.1u/10V_4
C20 C361 EV@10u/6.3V_6
C383 C115 C25 EV@0.1u/10V_4

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	N15P- DDR3 VRAM 1/2	1A
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EC 985LB1(KBC)
1.8V interface

1.8V p/n: AJ009850F02
Discription:IC CONTROLLER(128P)NPCE985LB1DX(LQFP)

985L-A0 connects to +3v / 985L-B1 connects to +1.8v

30mil

0.03A(30mils)

10mA

20140421:
Delete 1.05V_GFX_EN for Page.40

20140418:
Add VRON for Page.35

20140421:
Delete DGPU_PWROK

pin91 in 985L is 1.8V only

2014/04/21:
Delete GPIO66 DGPU_PWR_EN for +3V_GFX

<20090721_FAE suggestion>
Stuff 100K and close to EC side
for improving power consumption

Reserve for writing ME ROM

PECI interface should be used on Bay Trail platform,
thus VTT pin can wire to GND and PECI signal
can be left un-connected.

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU

985LB1 Pin88

20130606 Colay with 985L

SM BUS PU(KBC)

2013/07/31
SMBus Tr fail (spec 1000 ns max, result 1046 ns)
Change PU resister(R424,R428) from 10K to 4.7K

20140423:
Default use +3V

Q54 need Replacement at BOT layer.

Close to EC

HWPG(KBC)

20140421:
Change to HWPG_1.5V

<20130722>Change power from +3V to +3V_S5 for power sequence issue

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	NPCE885/FLASH	1A

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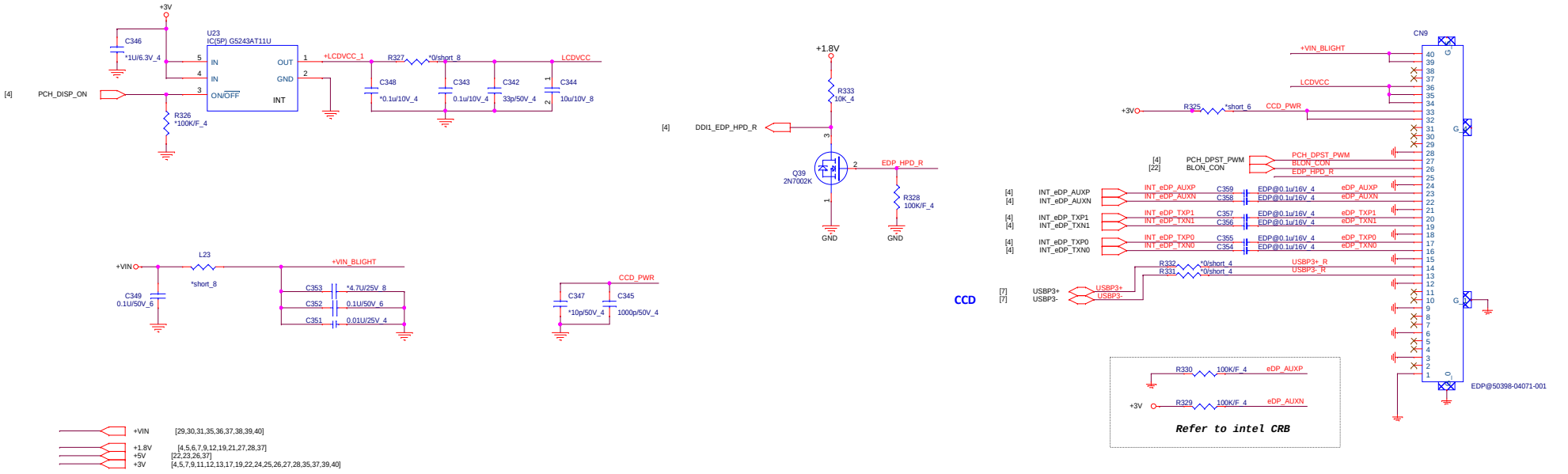
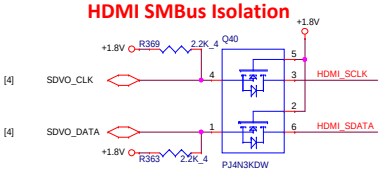
EDP Conn.

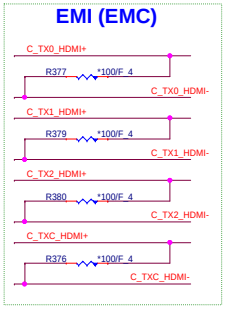


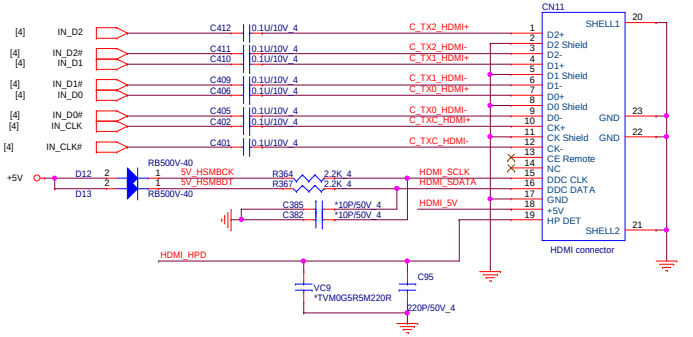
HDMI Conn.

HDMI SMBus Isolation



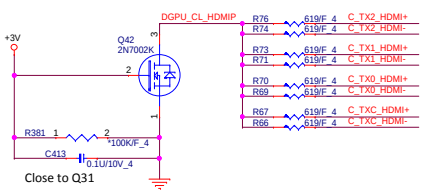
EMI (EMC)



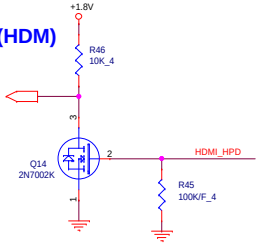


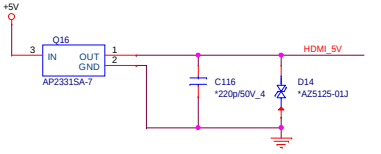
HDMI-Level shift (HDM)

Close to HDMI connector



HDMI-detect (HDM)





Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	LCD/HDMI/Camera	1A
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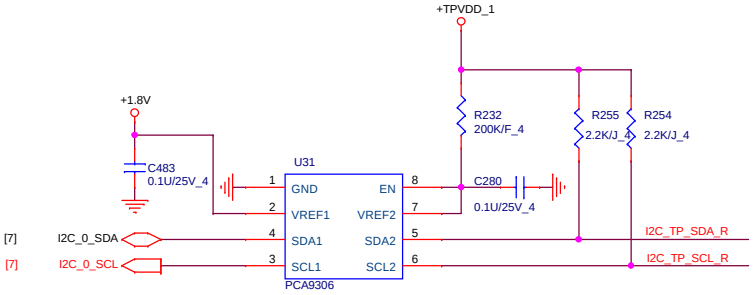
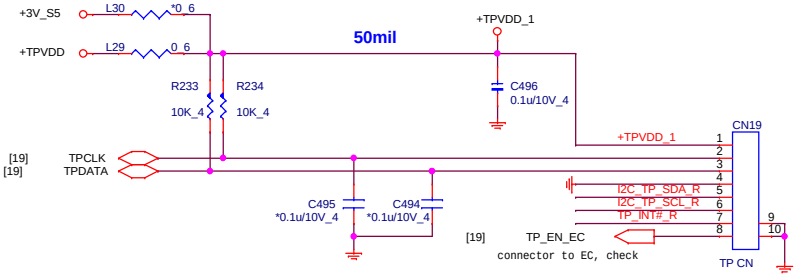
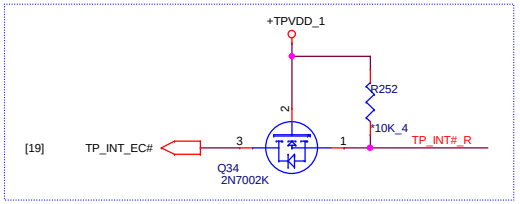
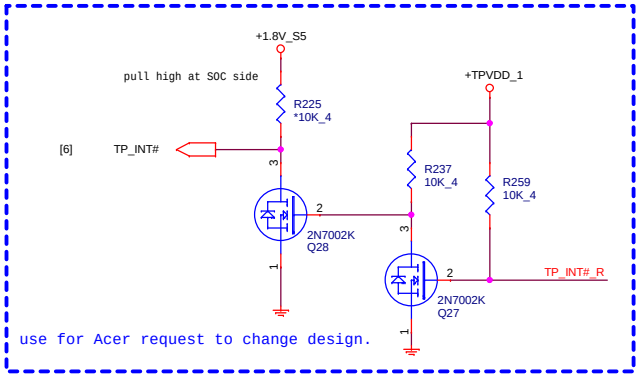
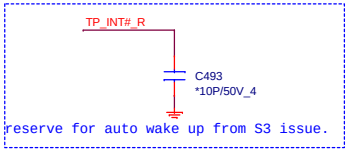
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)



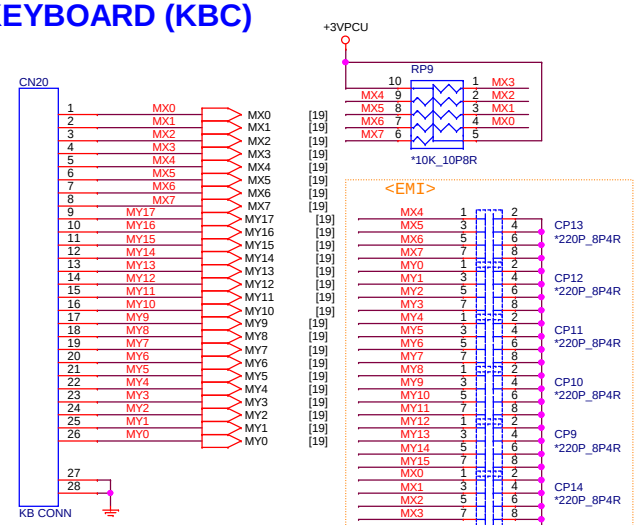


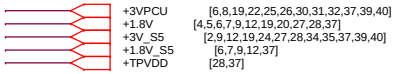






KEYBOARD (KBC)





Quanta Computer Inc.

PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	KB/BT/TP/LED/Power Connector	1A
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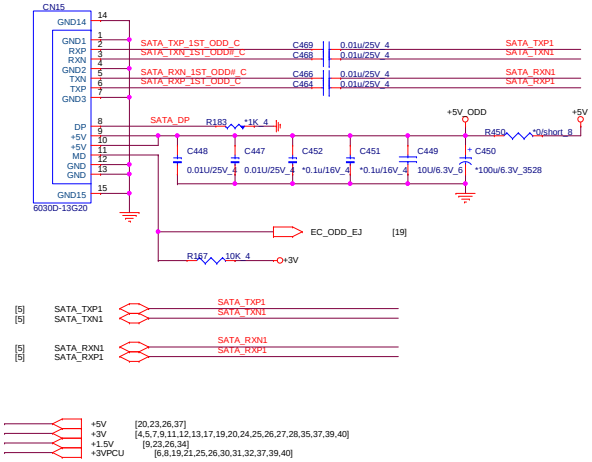
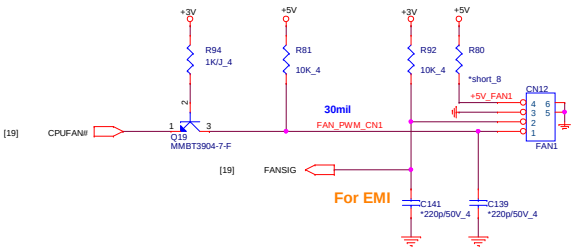
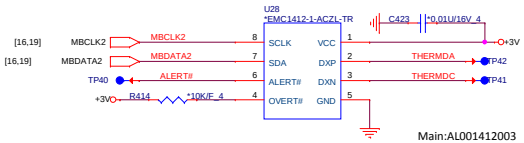
SATA ODD Connector



CPU FAN CTRL(THM)



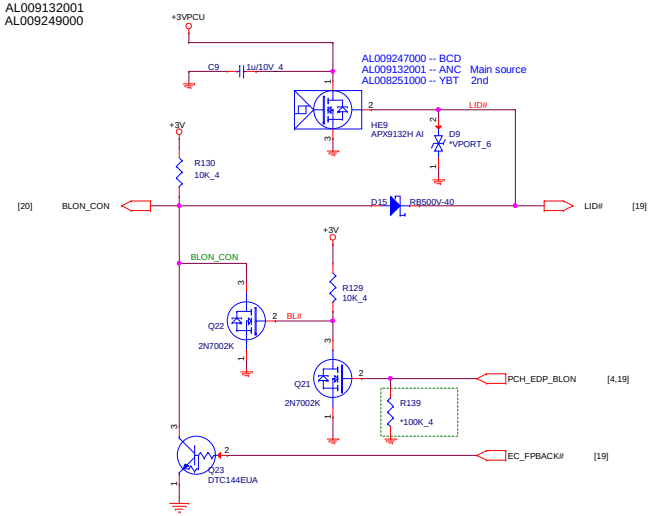
CPU Thermal sensor(THS) / MB Local TEMP



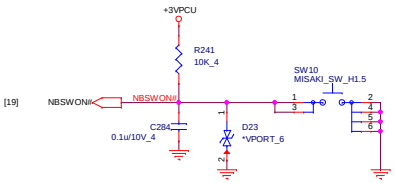
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

HALL IC (HSR)

1st source : EOD
2nd source : AL008251000 -- YBT
3rd source : AL009132001
4th source : AL009249000



Power Switch. (FSW)



Quanta Computer Inc.
PROJECT ZYL/ZYLA

Size	Document Number	Rev
	ODD/FAN/Hall/PSW	1A

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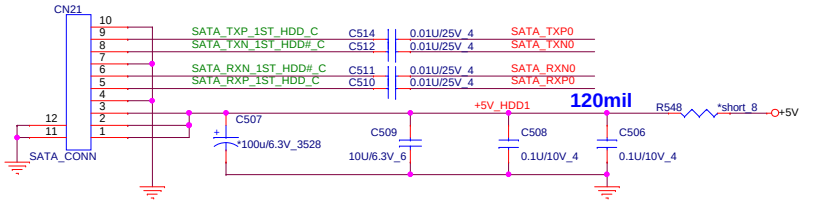
SATA HDD1

HDD1



[5] SATA_TXP0 — SATA_TXP0
[5] SATA_TXN0 — SATA_TXN0

[5] SATA_RXN0 — SATA_RXN0
[5] SATA_RXP0 — SATA_RXP0

+5V [20,22,26,37]
+1.5V [9,22,26,34]

Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	SATA HDD/SATA REDRIVER	1A

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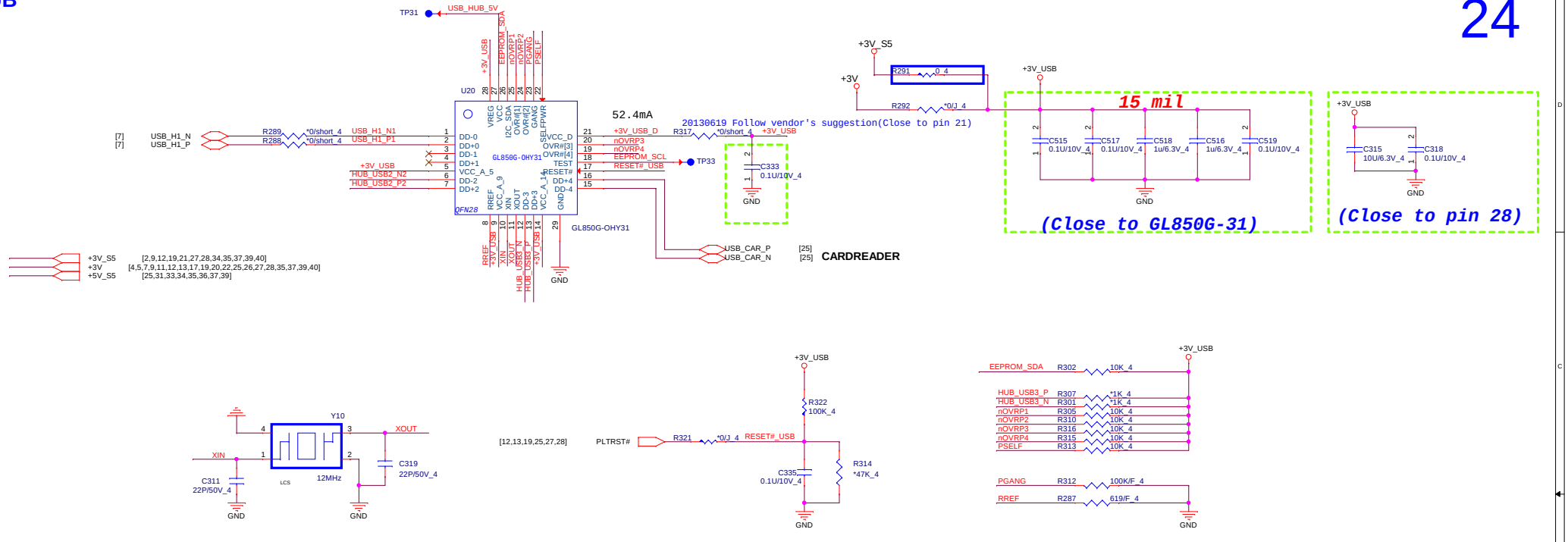
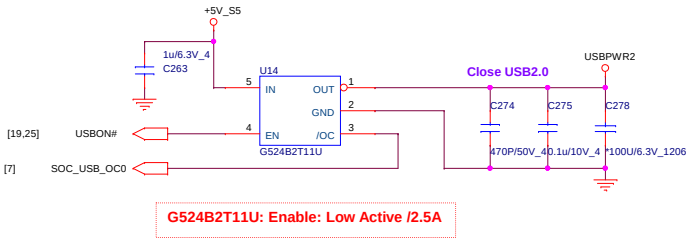
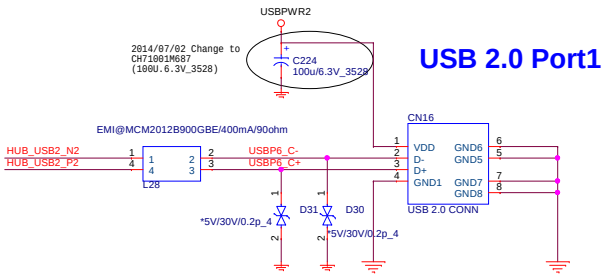
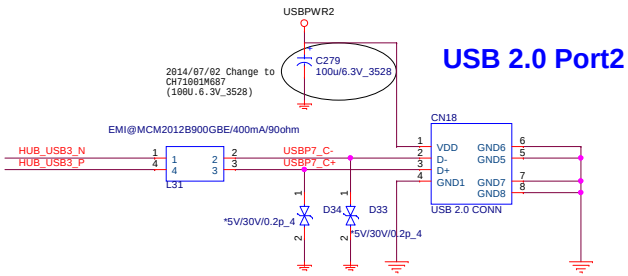
USB HUB



USB 2.0 CONNECTOR X2







Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	USB BOARD CONN	1A
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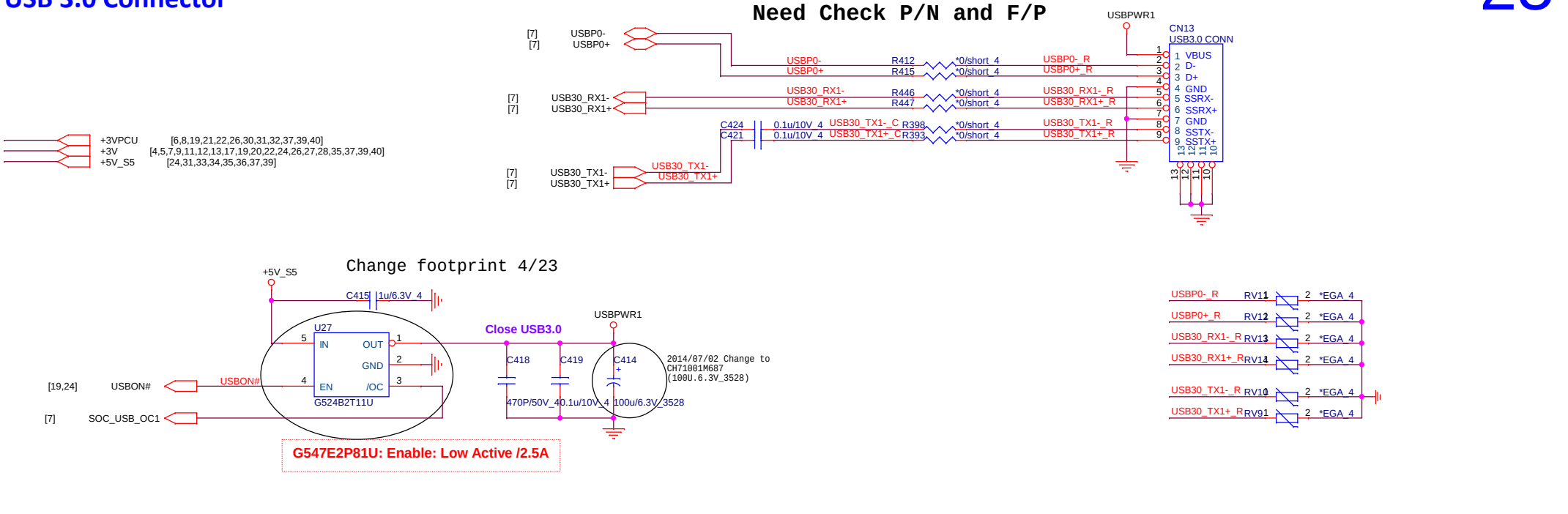
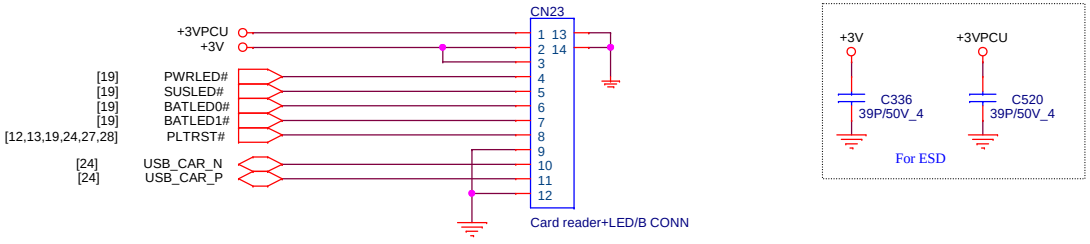
USB 3.0 Connector



Card Reader+ LED/B Connector



Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	USB 3.0 / Card Reader+LED CONN	1A
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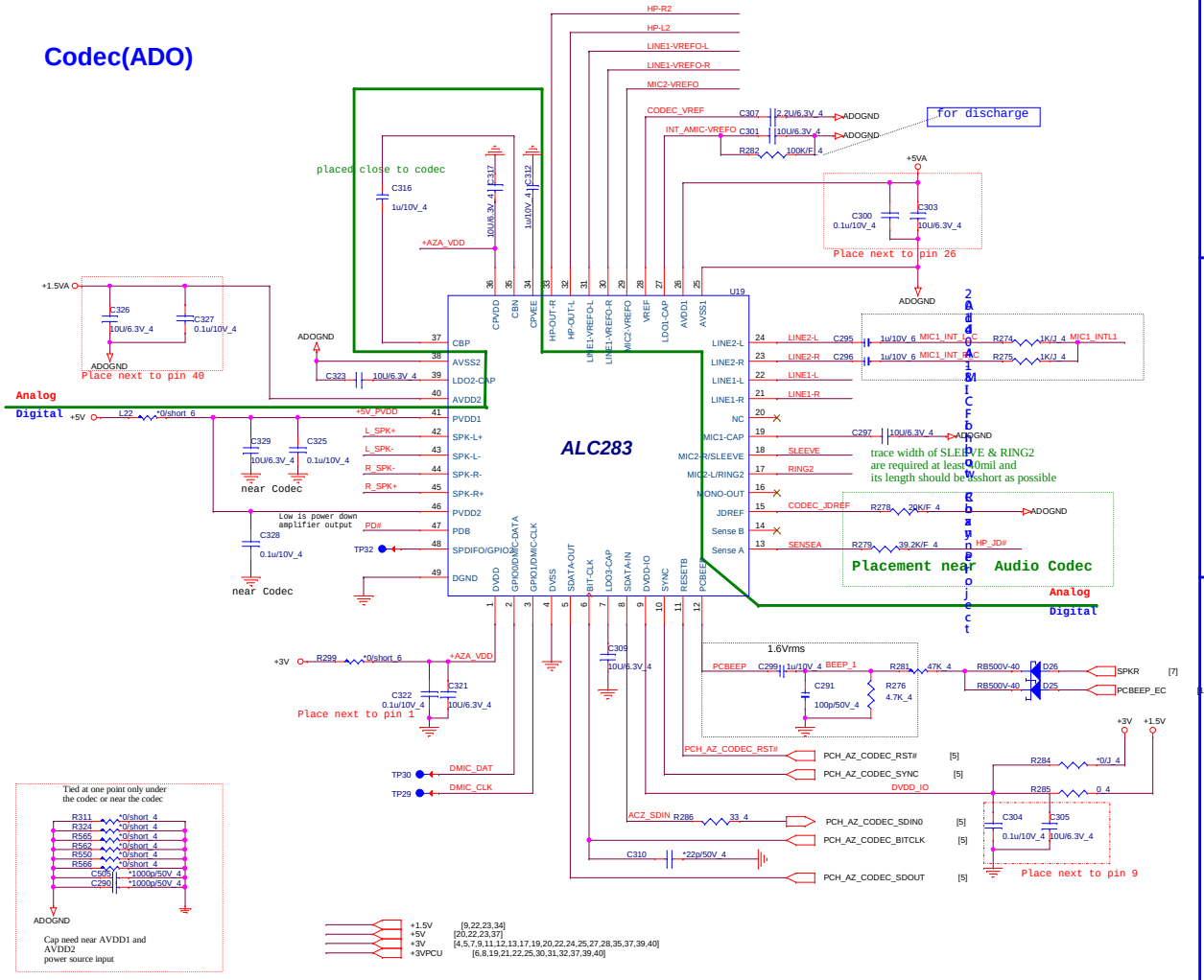
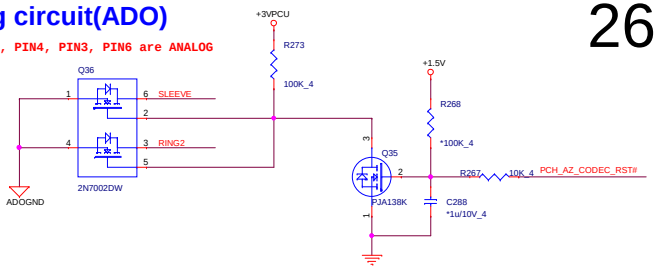
Codec(ADO)

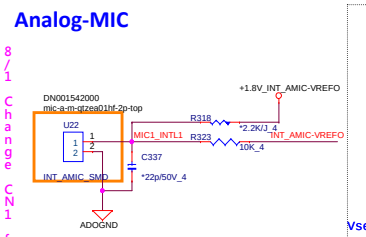


Grounding circuit(ADO)

PIN1, PIN4, PIN3, PIN6 are ANALOG

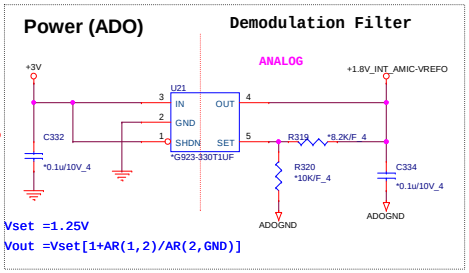


Analog-MIC



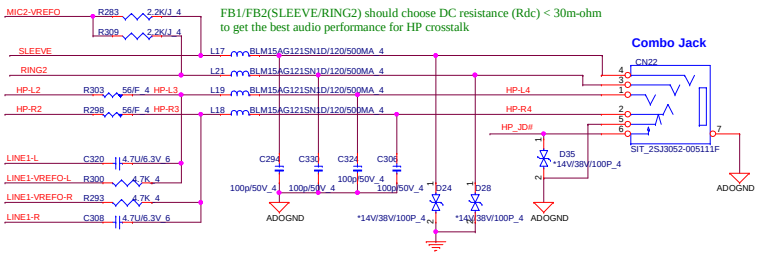
Power (ADO)

Demodulation Filter

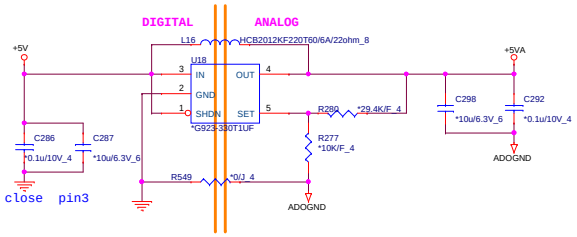


HEADPHONE/MIC/LINE combo (AMP)

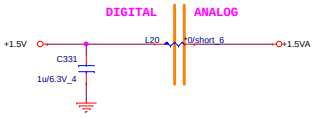
FB1/FB2(SLEEVE/RING2) should choose DC resistance (Rdc) < 30m-ohm to get the best audio performance for HP crosstalk



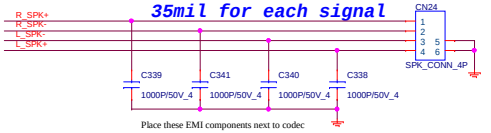
Codec PWR 5V(ADO)



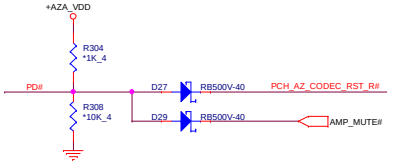
Codec PWR 1.5V(ADO)



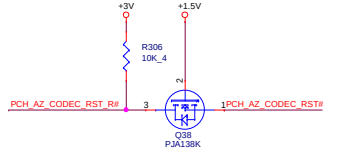
Internal Speaker



Mute(ADO)



Level shift



Quanta Computer Inc. PROJECT : ZYL/ZYLA		
Size	Document Number: Codec ALC3225	Rev: 1A
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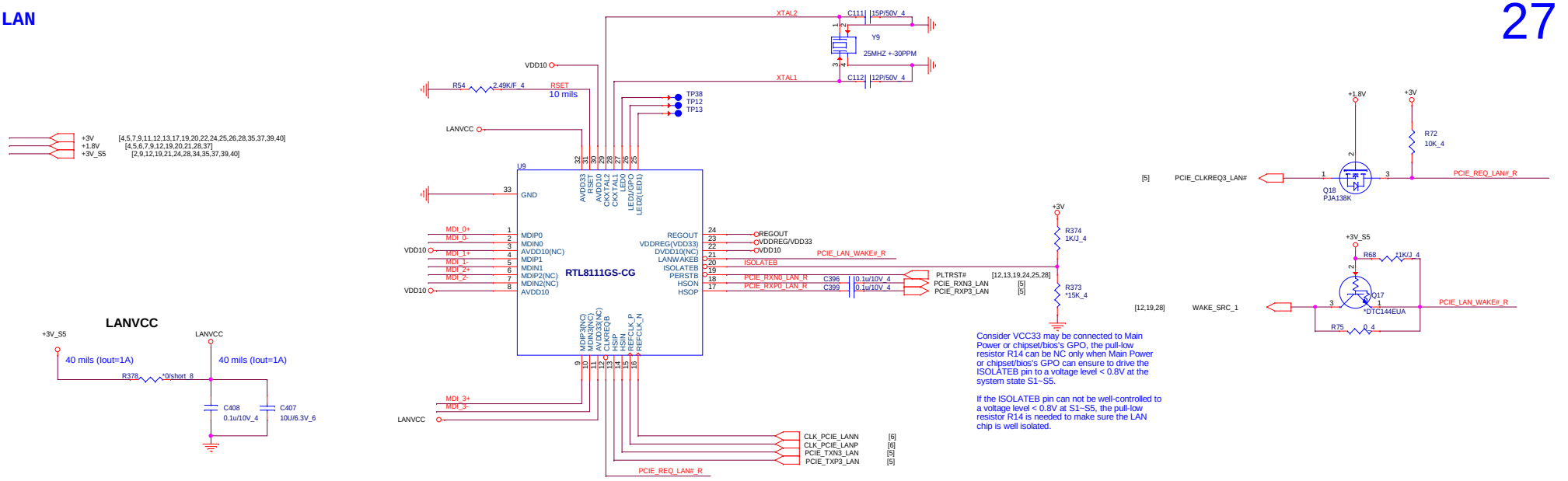
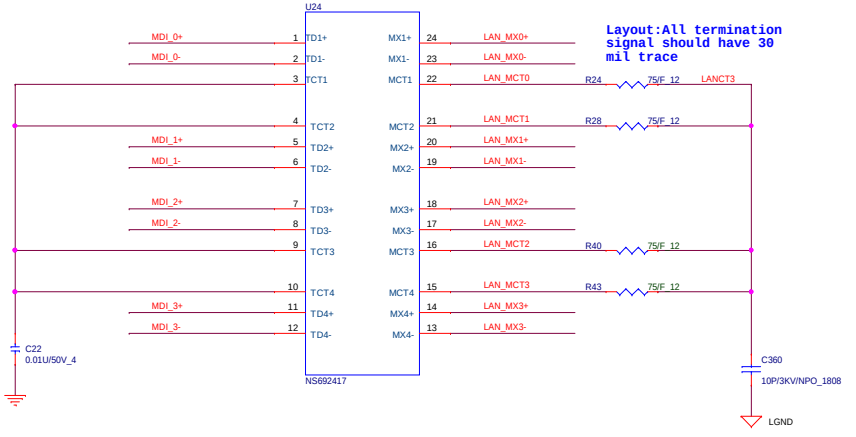
LAN

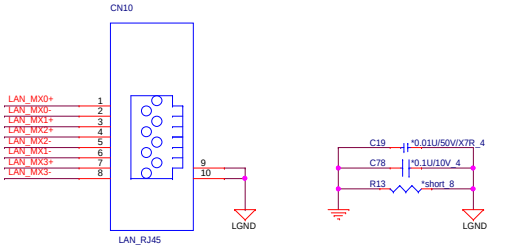


Tramsformer



RJ45 Connector

Need Check P/N and F/P



Quanta Computer Inc.		
PROJECT : ZYL/ZYLA		
Size	Document Number: LAN	Rev: 1A
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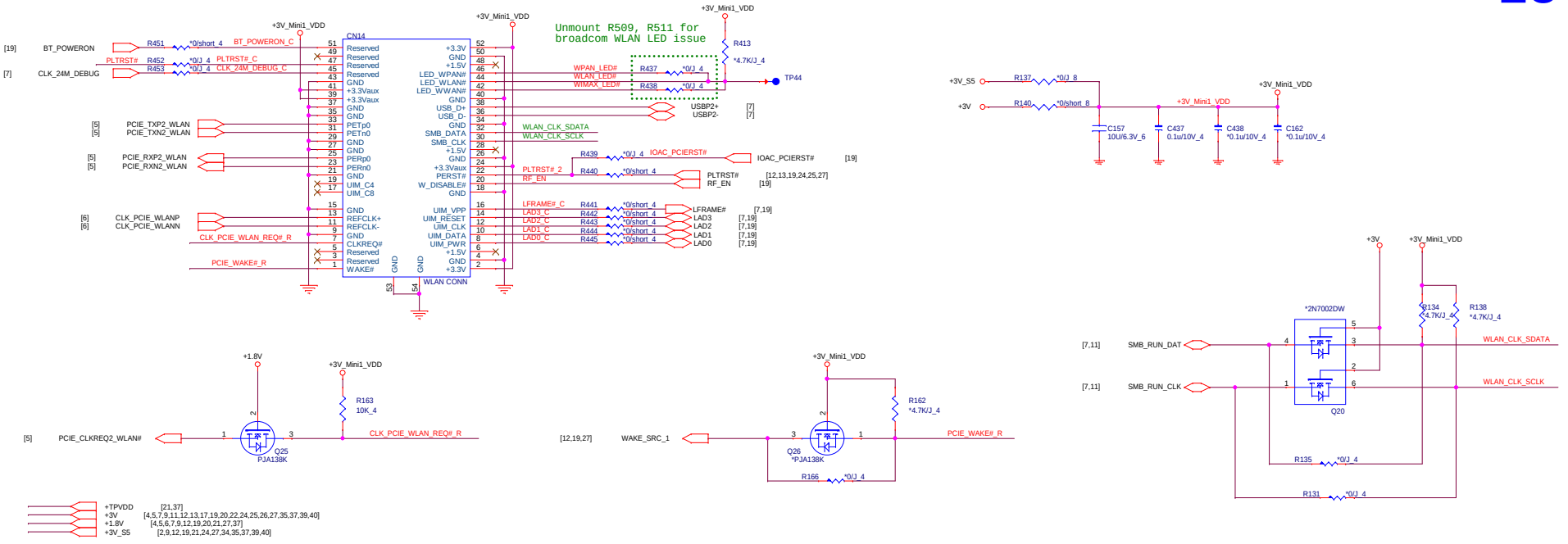
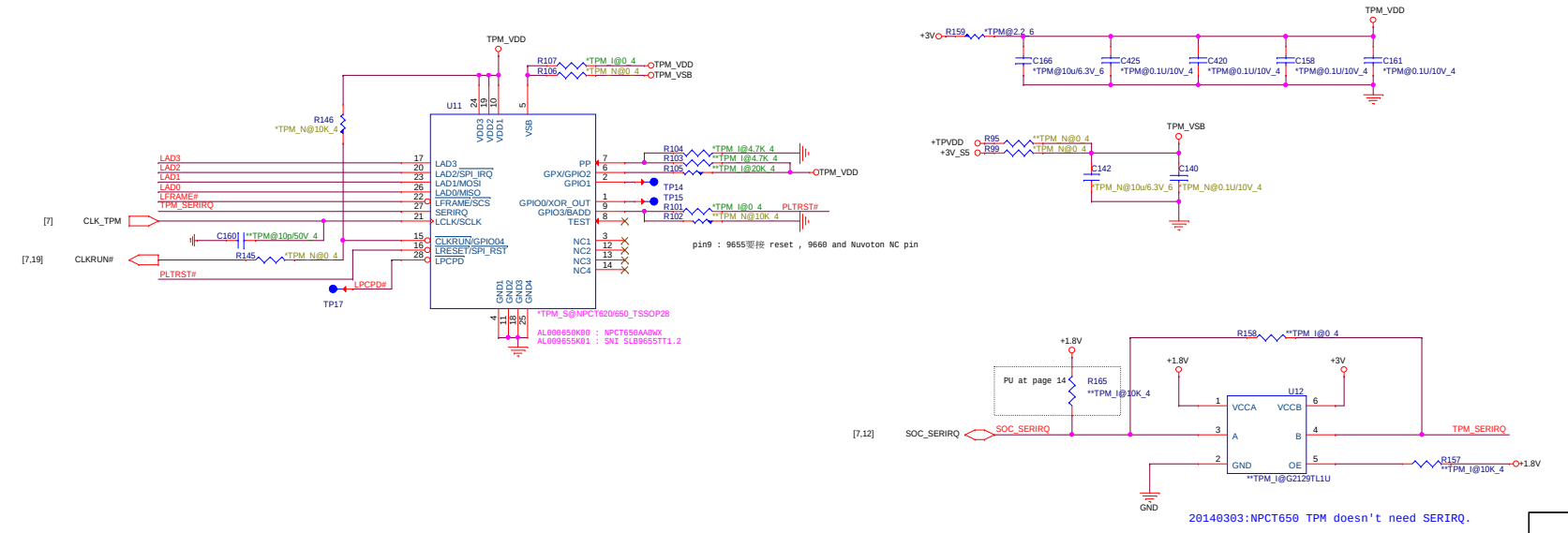
WLAN



TPM (TPM)



Quanta Computer Inc. PROJECT : ZYL/ZYLA			
Size	Document Number: WiFi & BT & TPM		Rev: 1A
Date: Thursday, July 10, 2014	Sheet 28 of 44		

HOLE(OTH)

HOLE20 *H-C315D110P2

HOLE22 *HG-C315D110P2

HOLE23 *HG-C315D110P2

HOLE27 *HG-C315D110P2

HOLE25 *HG-C315D110P2

HOLE15 *HG-C315D110P2

HOLE14 *H-C110D110N

HOLE24 *HG-C315D110P2

HOLE28 *H-C315D110P2

HOLE29 *hg-tc315bc236d110p2

HOLE13 *HG-C315D110P2

HOLE18 *H-C315D110P2

HOLE12 *HG-C315D110P2-V5

HOLE26 *HG-C315D110P2

GPU nuts

HOLE16 EV@H-C236D138P2

HOLE19 EV@H-C236D138P2

HOLE17 EV@H-TC236I138BC236D138P2

Mini card nuts

HOLE21 H-C217D61P2

CPU nuts

HOLE9 *H-TC256BC236D161P2

HOLE10 *H-TC256BC236D161P2

HOLE11 *H-TC256BC236D161P2

reserve for ESD

C522 0.1U/25V_4 +1.05V_GFX

C523 0.1U/25V_4 +VA_IACM

C524 0.1U/25V_4 +3V

C258 0.1U/25V_4 +3V

C302 0.1U/25V_4 +5V_S5

+3VPCU C285 0.1U/25V_4 +5V_S5

0.1U/25V_4 C143 +3VPCU

+VCC_CORE C212 *0.1U/10V_4 +VCC_GFX

C205 *1000p/50V_4

+VA_IACM C429 *0.1U/25V_4 +VIN

C428 *1000p/50V_4

C262 *0.1U/25V_4 +VIN

C47 *1000p/50V_4

C430 2.2n/50V_6 +VA_IACM

Quanta Computer Inc.

PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	USB BOARD CONN	1A
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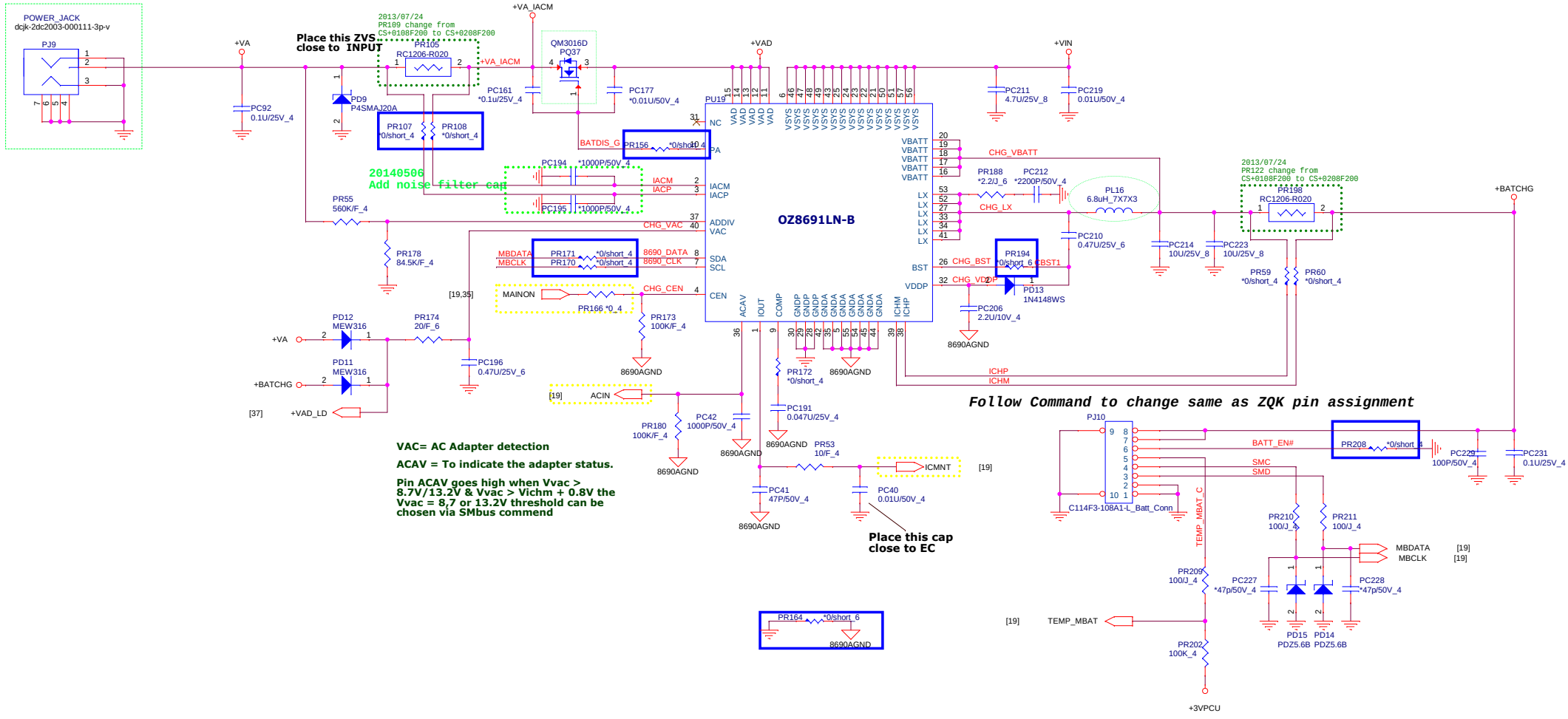
DFPJ06MR013-- 95W
DFPJ06MR007--- 45W

ZE7



Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: Charger (OZ8690ALN)	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 30 of 44	

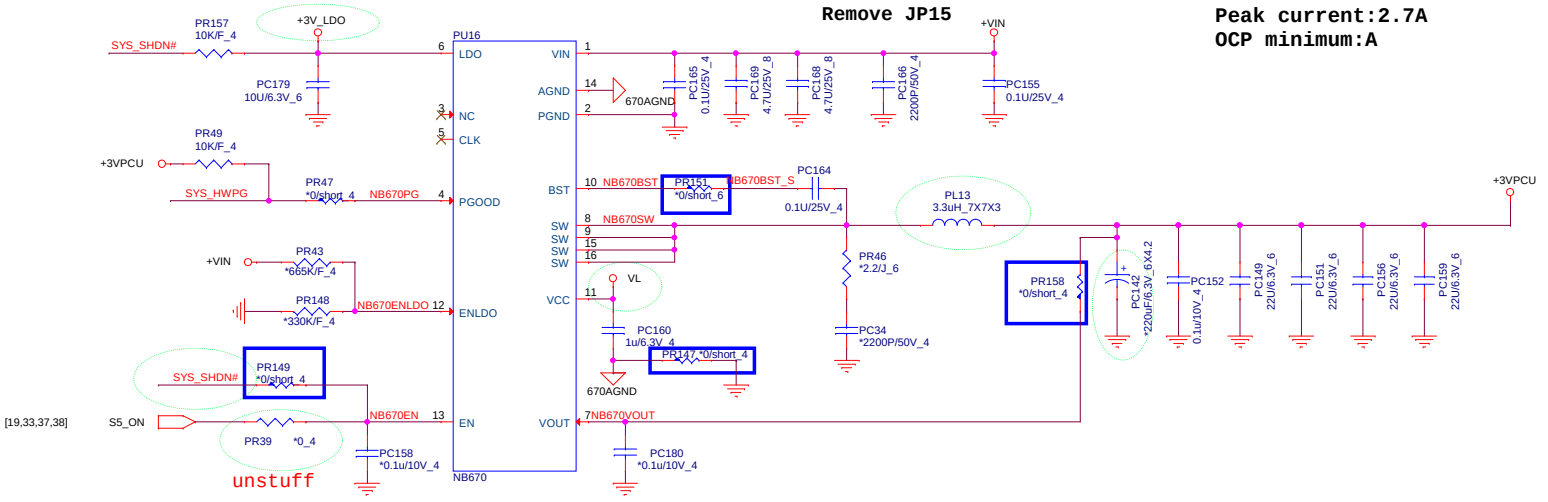
DC/DC +3VPCU/+5V_S5

+3VPCU [6,8,19,21,22,25,26,30,32,37,39,40]
+5V_S5 [24,25,33,34,35,36,37,39]
SYS_SHDN# [32,38]

LDO(MAX)=100mA

Remove JP15

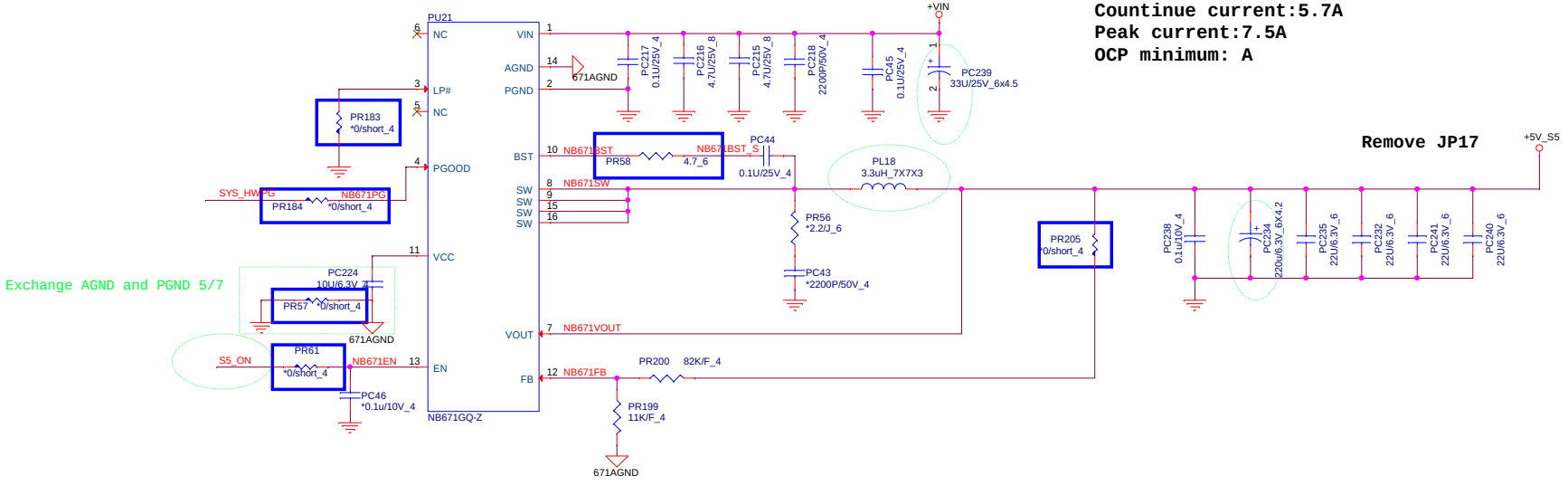
+3.3 Volt +/- 5%
Countinue current:2A
Peak current:2.7A
OCP minimum:A



Remove JP13

Remove JP18

+5 Volt +/- 5%
Countinue current:5.7A
Peak current:7.5A
OCP minimum: A



Exchange AGND and PGND 5/7

Remove JP17

Quanta Computer Inc.
PROJECT : ZHJ

Size	Document Number	Rev
	3/5VS5 (NB670/NB669)	1A
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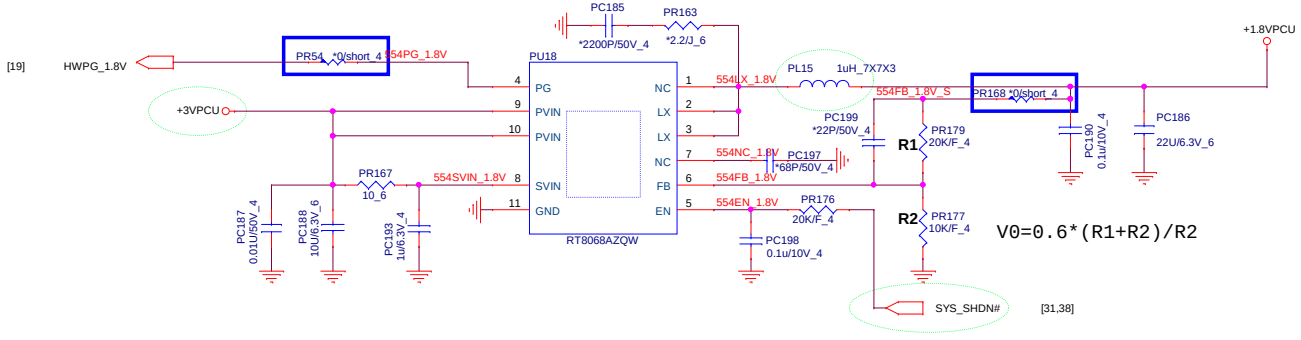
[12,19,37] +1.8VPCU

[6,8,19,21,22,25,26,30,31,37,39,40] +3VPCU

+1.8V Volt +/- 5%
Countinue current:0.08A
Peak current:0.11A
OCP minimum:A



removed PR161 and PR165

Quanta Computer Inc.			
PROJECT : ZHJ			
Size	Document Number +1.8VPCU		Rev 1A
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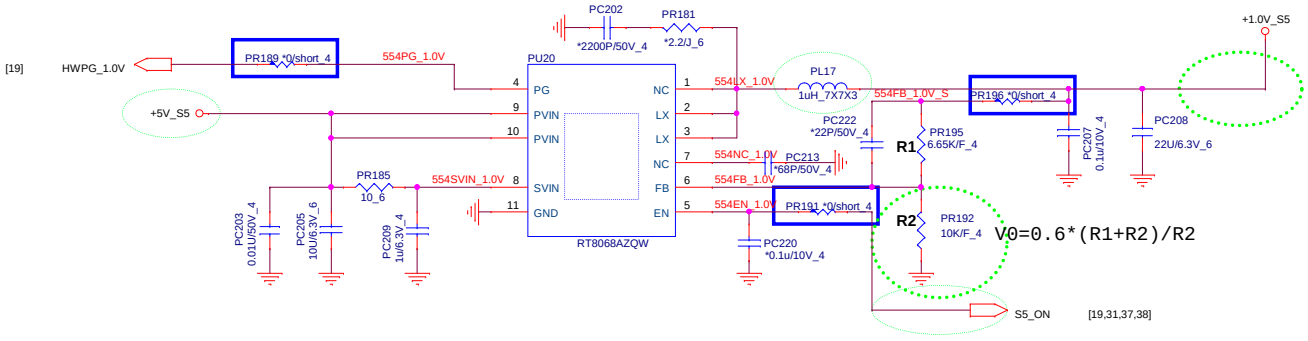
[9,37] +1.0V_S5
[24,25,31,34,35,36,37,39] +5V_S5
[2,9,12,19,21,24,27,28,34,35,37,39,40] +3V_S5

+1.0V Volt +/- 5%
Countinue current:2.4A
Peak current:3.2A
OCP minimum:A



removed PR169 ,PR175 and PR182

V0=0.6*(R1+R2)/R2

20140609:
Change PR192 from 10K to 9.31K Ohm

Quanta Computer Inc.
PROJECT : ZHJ

Size	Document Number	Rev
	+1.0V	1A
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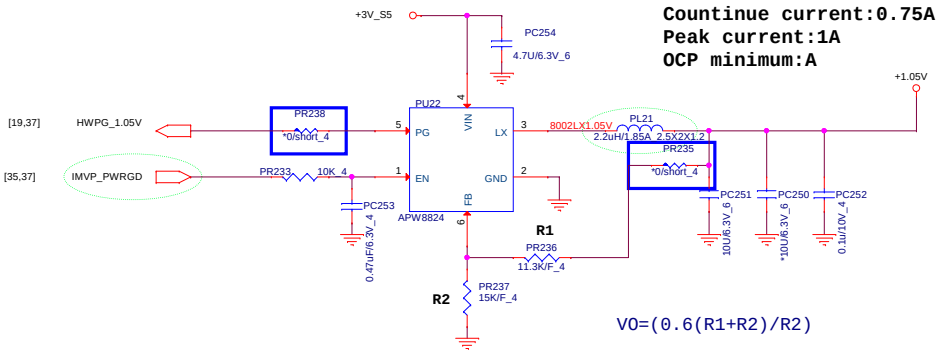
[2,9,12,19,21,24,27,28,35,37,39,40] +3V_S5

[5,9] +1.05V

[9,22,23,26] +1.5V

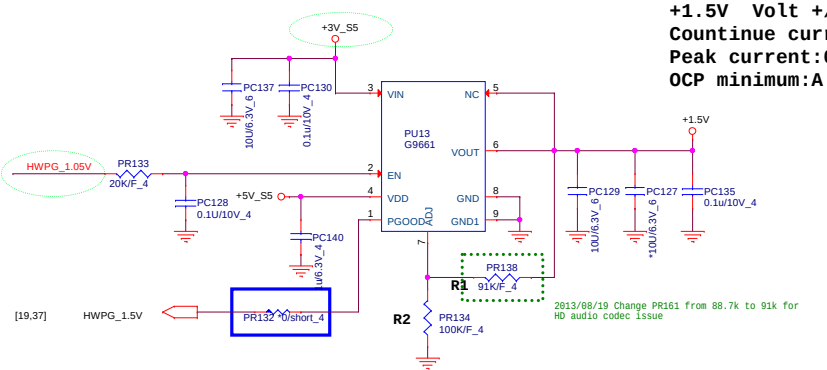
+1.05V Volt +/- 5%
Countinue current:0.75A
Peak current:1A
OCP minimum:A



removed PR232 and PR234

VO=(0.6(R1+R2)/R2)

+1.5V Volt +/- 5%
Countinue current:0.023A
Peak current:0.03A
OCP minimum:A



2013/08/19 Change PR161 from 88.7k to 91k for HD audio codec issue

VO=(0.8(R1+R2)/R2)
R2<120Kohm

Quanta Computer Inc.
PROJECT : ZHJ

Size	Document Number	Rev
	+1.05V/1.5V	1A

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20130617 Change +1.05V to +1.05V

Close to VR

VR_SVID_ALERT# close to CPU

VR_SVID_DATA and VR_SVID_CLK close to VR

[6,9,37] +1.0V
[8,9,29] +VCC_GFX
[20,29,30,31,36,37,38,39,40] +VIN
[24,25,31,33,34,36,37,39] +5V_S5

Parallel

Close to the CPU side.

PU9 ISL95833HRTZ-T

AXG

Remove JP19

+VCC_GFX
TDC : A
PEAK : 14A
OCP : A
Width : mil

GFX_CORE Load Line : -5.9mV/A for 2.xW SDP

DCR=4.2mOhm

Close to the VR side.

Close with AXG inductor

Core

Remove JP20

+VCC_CORE
TDC : A
PEAK : 12A
OCP : A
Width : mil

VCORE Load Line : -5.9mV/A for 2.xW SDP

Close with phase1 inductor

Quanta Computer Inc.
PROJECT : ZHJ

Size | Document Number: +VCC_CORE/+VGFX (ISL95833) | Rev 1A
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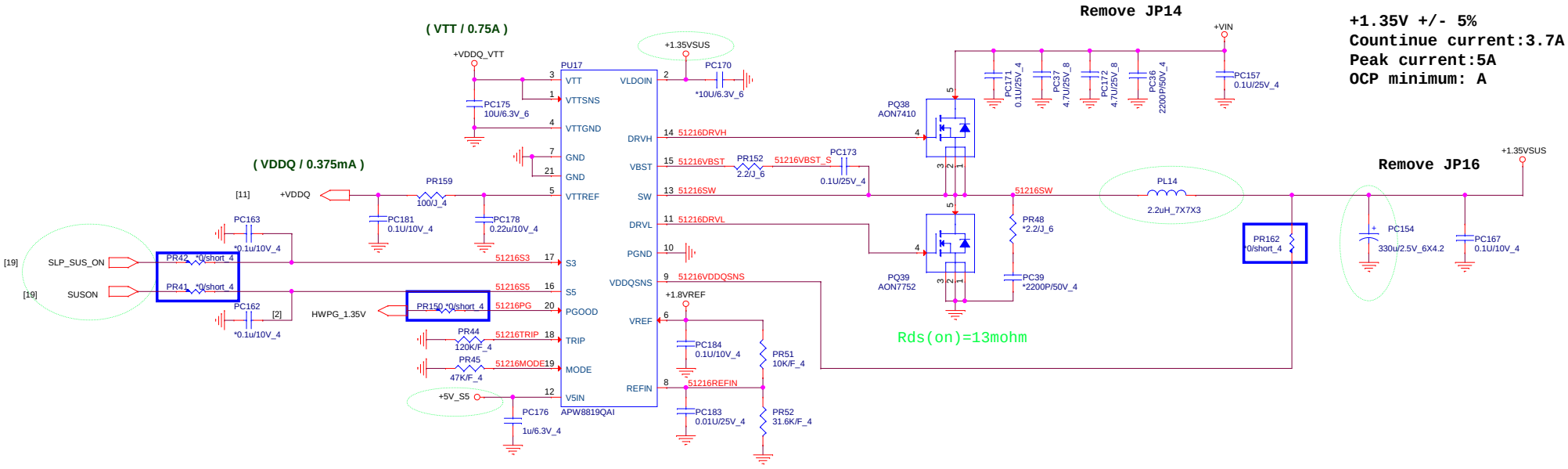
[2,8,11,37] +1.35VSUS

[11] +VDDQ_VTT

[24,25,31,33,34,35,37,39] +5V_S5



Quanta Computer Inc.			
PROJECT : ZHJ			
Size	Document Number		Rev
	DDR3 (APW8819)		1A
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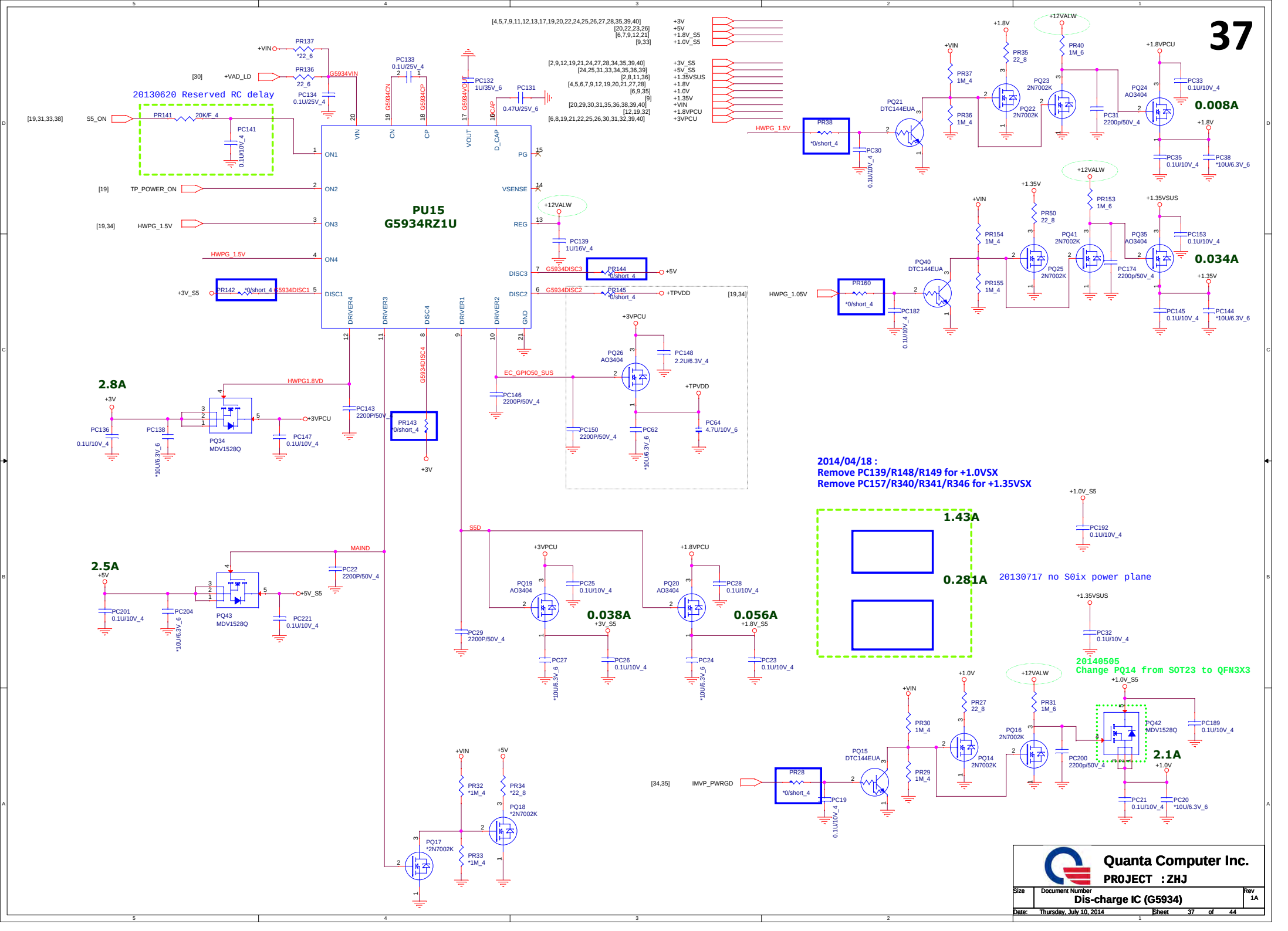
20130620 Reserved RC delay
PU15
G5934RZ1U
2.8A
2.5A
1.43A
0.281A
0.038A
0.056A
0.008A
0.034A
2.1A
2014/04/18 :
Remove PC139/R148/R149 for +1.0VSX
Remove PC157/R340/R341/R346 for +1.35VSX
20130717 no S0ix power plane
20140505
Change PQ14 from SOT23 to QFN3X3
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PROJECT : ZHJ
Dis-charge IC (G5934)
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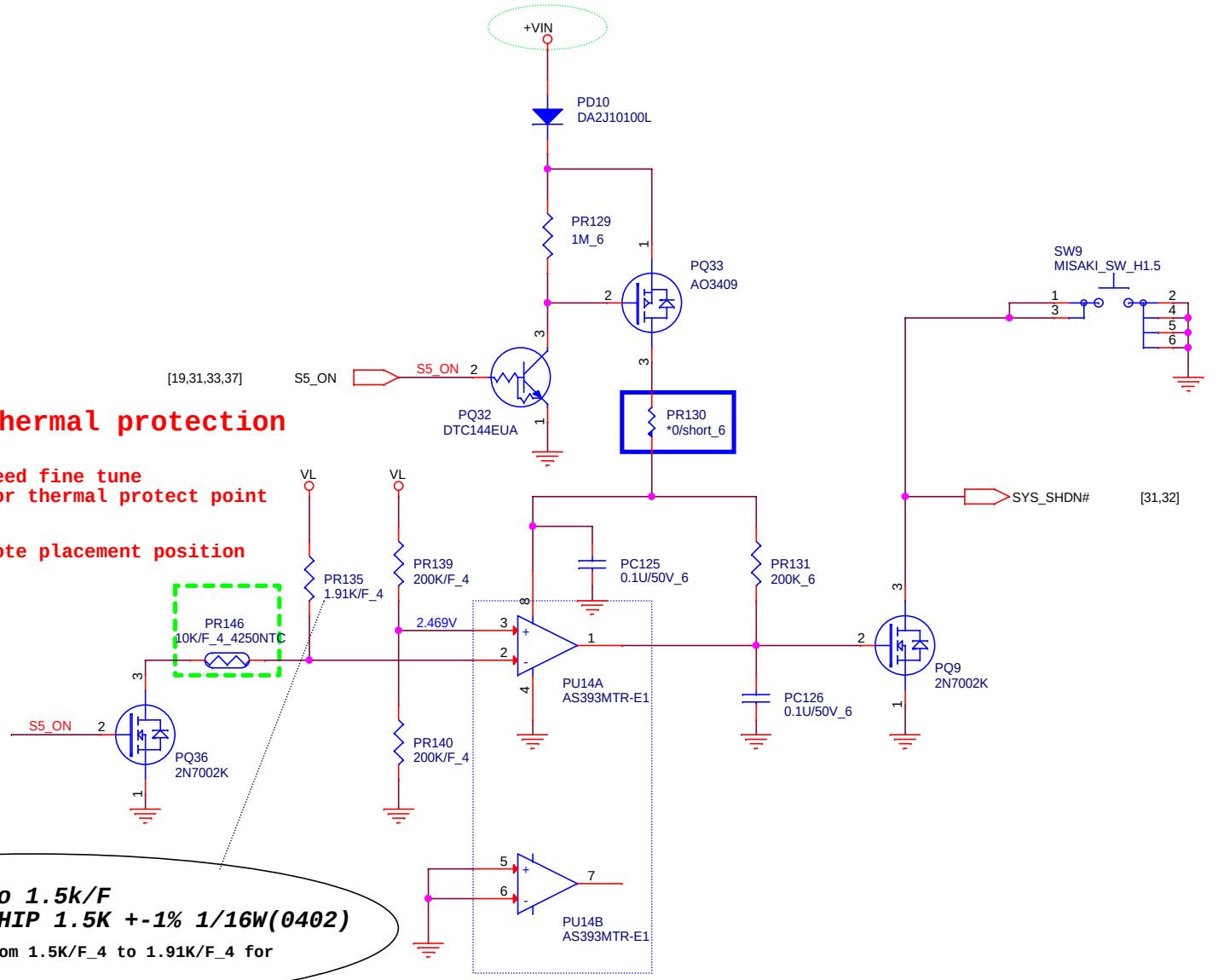

note: PR173 change to 1.5k/F
CS21502FB14 RES CHIP 1.5K +-1% 1/16W(0402)

20140702 Change PR135 from 1.5K/F_4 to 1.91K/F_4 for thermal request

For EC control thermal protection (output 3.3V)

Quanta Computer Inc.		
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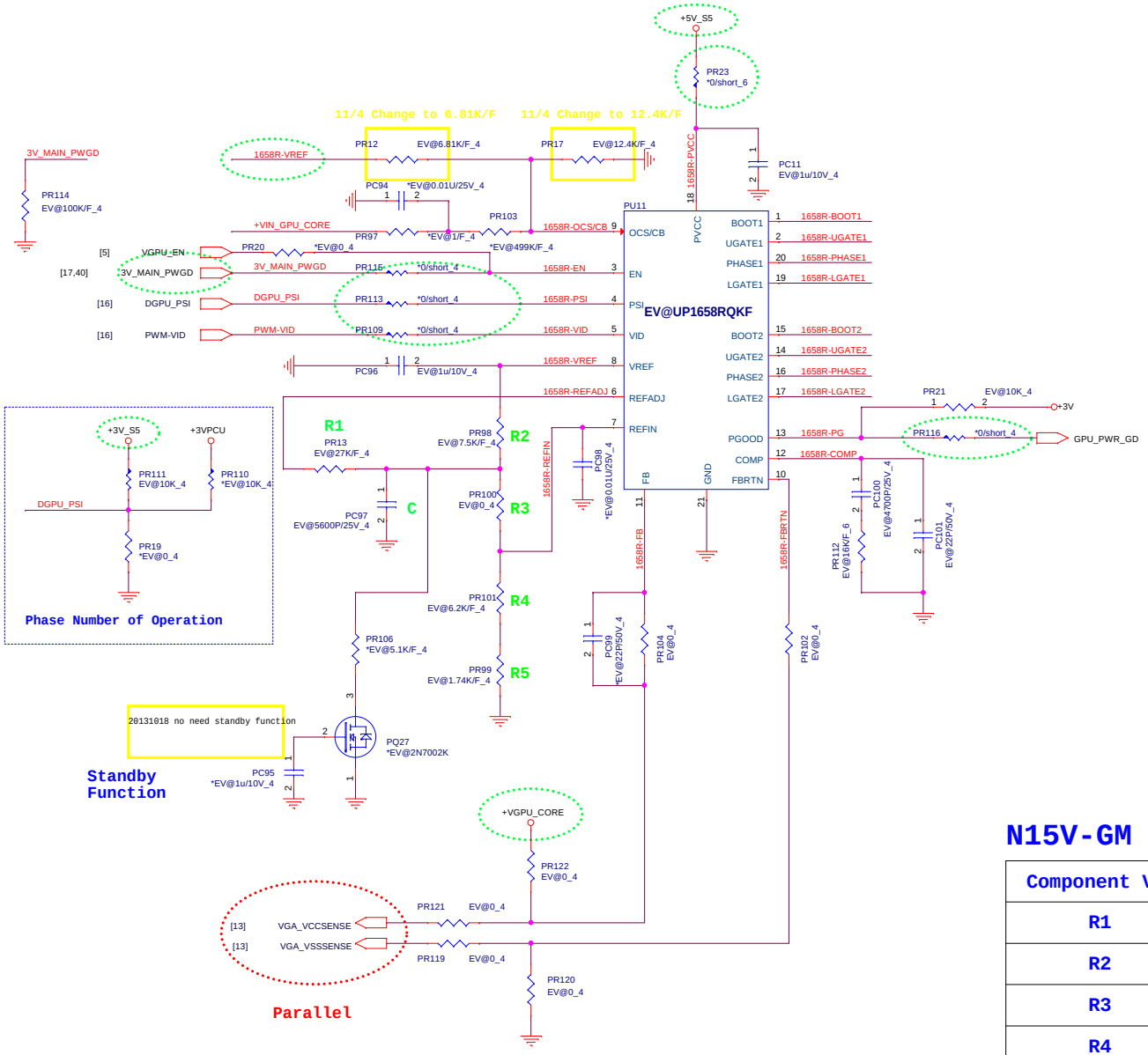

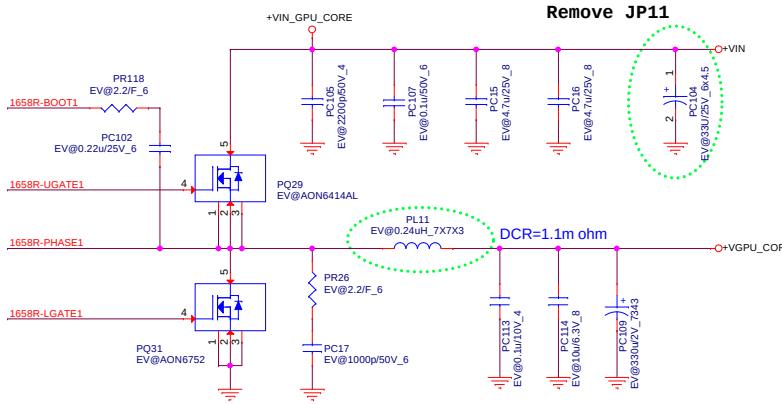

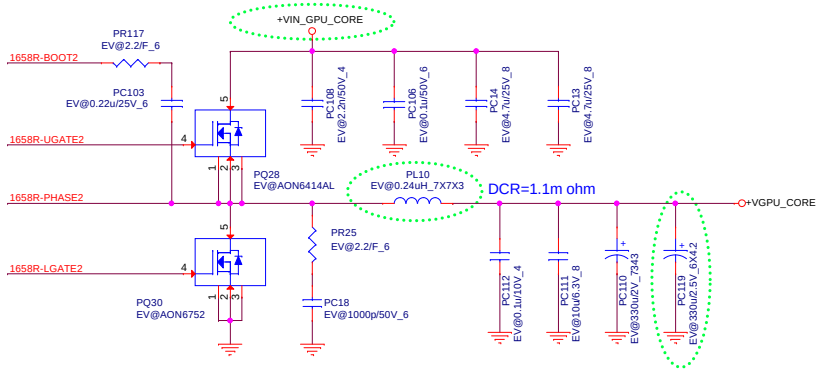

N15V-GM

Component Value	Config D
R1	27K
R2	7.5K
R3	0
R4	6.2K
R5	1.74K
C	5.6nF

N15V-GM

+VGPU_CORE
Countinue current:33.5A
Peak current:51.5A
OCP:75A
FSW:300KHz
L/L=0mV/A

Quanta Computer Inc.
PROJECT : ZQ0

Size	Document Number	Rev
	+VGPU_CORE (UP1658RQKF)	1A
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[13,14,15] +1.05V_GFX
[13,14,18] +1.5V_GFX
[13,16,17] +3V_GFX

+1.05V_GFX
TDC : 1.553A
PEAK : 2.29A
Width : 90mil

20140421:
Change 554PG_1.05V to Test PAD.

Remove JP12

Remove JP14

PU12 EV@RT8068AZQW

20140529:
Change PR125 from 10K to 26.7K Ohm
V0=0.6*(R1+R2)/R2

20140421:
Change Enable from 3V_MAIN_PWRGD

+3V_GFX
TDC : 0.17A
PEAK : 0.342A
Width : 20mil

Remove JP9

20140606:
modify +1.5V_GFX PG sequence

20140609:
Change PL9 from 3.3uH to 2.2uH

Remove JP10

+1.5V_GFX
1.5 Volt +/- 5%
TDC : 3.24A
PEAK : 4.25A
Width : 170mil

Change to 1.35V_GFX

PU10 EV@NB671

VREF=0.604V

20140606:
modify +1.5V_GFX PG sequence

20140709 Change PR9 from 54.9K to 66.5K for EMI request and +1.5V_GFX will Change to 1.35V_GFX

Quanta Computer Inc.
PROJECT : ZQ0
Size | Document Number: +1.5V_GFX/+1.05V_GFX/+3V_GFX | Rev 1A
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Bay Trail-M Power On Timing without S0ix (G3 to S0)

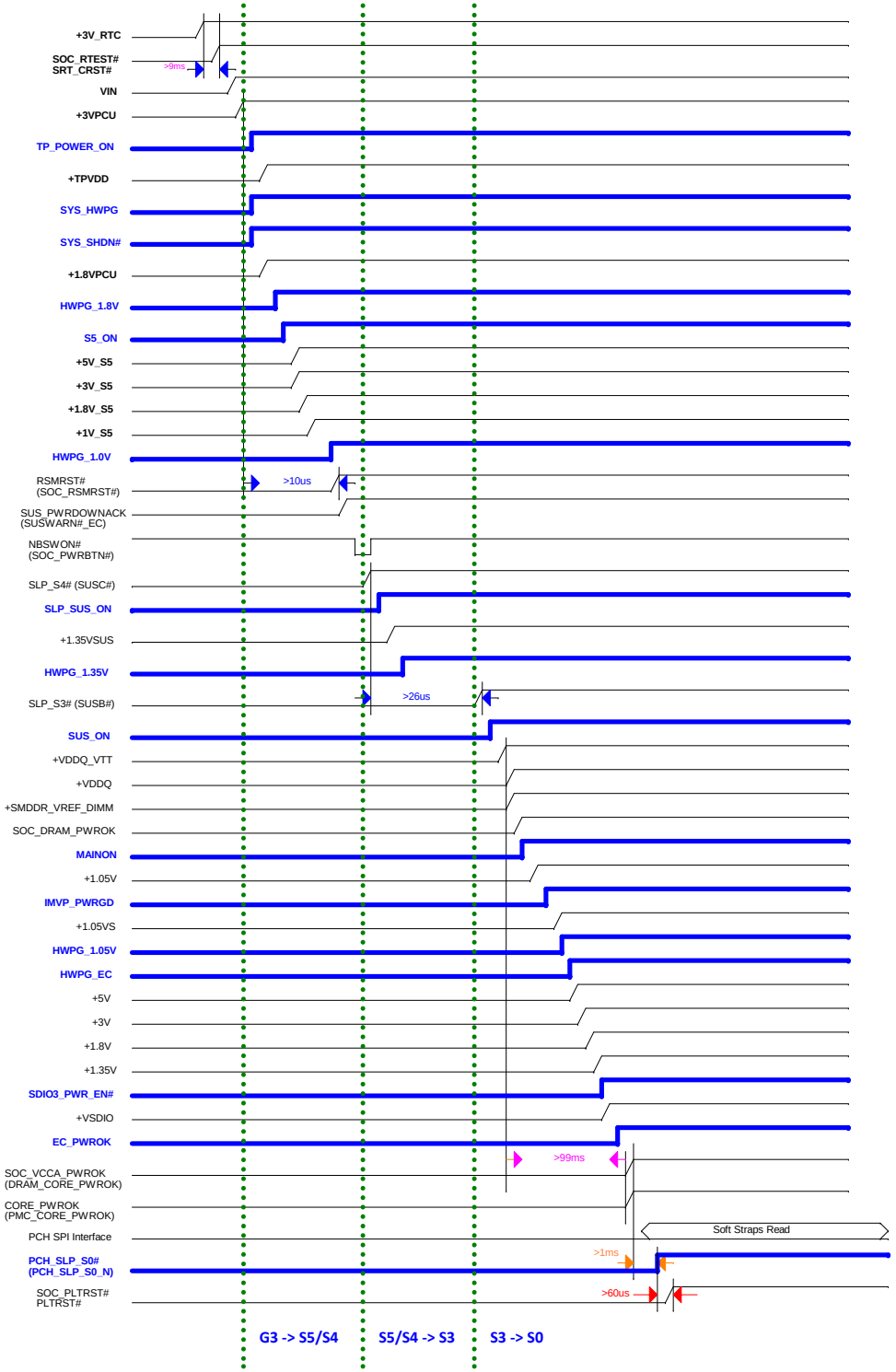
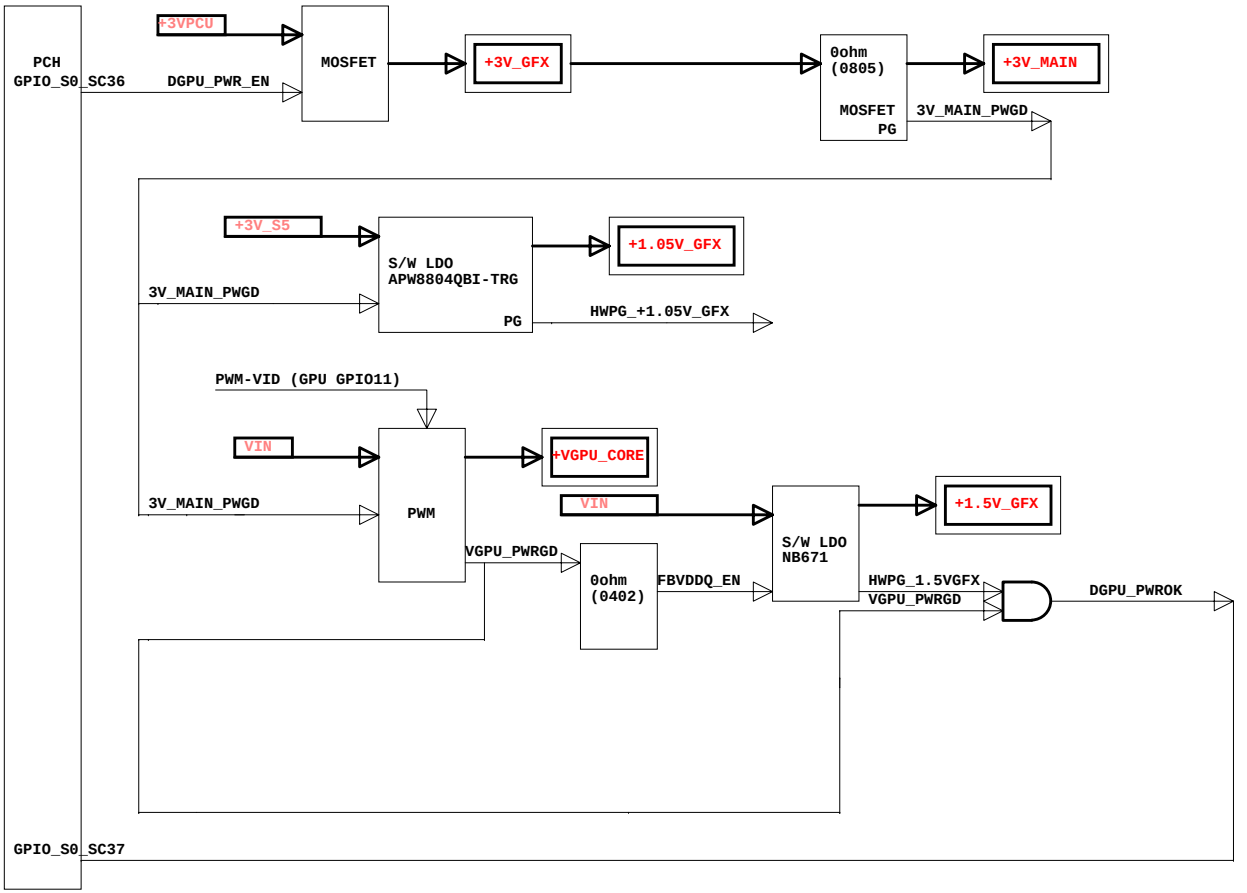


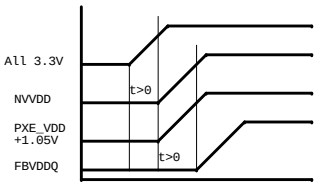
Table 37. SoC Sx-States to SLP_S*#

State	S0	S3	S4	S5	Reset w/o Power Cycle	Reset w/ Power Cycle
CPU Executing	In C0	OFF	OFF	OFF	No	OFF
PMC_SLP_S3#	HIGH	LOW	LOW	LOW	HIGH	LOW
PMC_SLP_S4#	HIGH	HIGH	LOW	LOW	HIGH	LOW
S0 Power Rails	ON	OFF	OFF	OFF	ON	OFF
PMC_PLTRST#	HIGH	LOW	LOW	LOW	LOW	LOW
PMC_SUS_STAT#	HIGH	LOW	LOW	LOW	HIGH	LOW
PCIe Links	L0, L1	L3	L3	L3	L3 Ready	L3

NOTES: The processor treats S4 and S5 requests the same. The processor does not have PMC_SLP_S5#. PMC_SUS_STAT# is required to drive low (asserted) even if core well is left on because PMC_SUS_STAT# also warns of upcoming reset.

VGA power up sequence

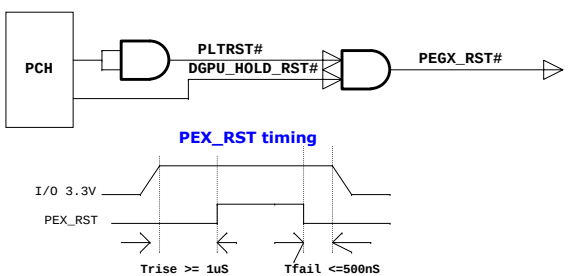




N15x Power on sequance

Notes: -All 3.3V includes all rails powered at 3.3V
-PEX_VDD 1.05V inculdes all rails that are shared

VGA Reset



Quanta Computer Inc.
PROJECT : ZYL

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	GPU PWR CRL	1A

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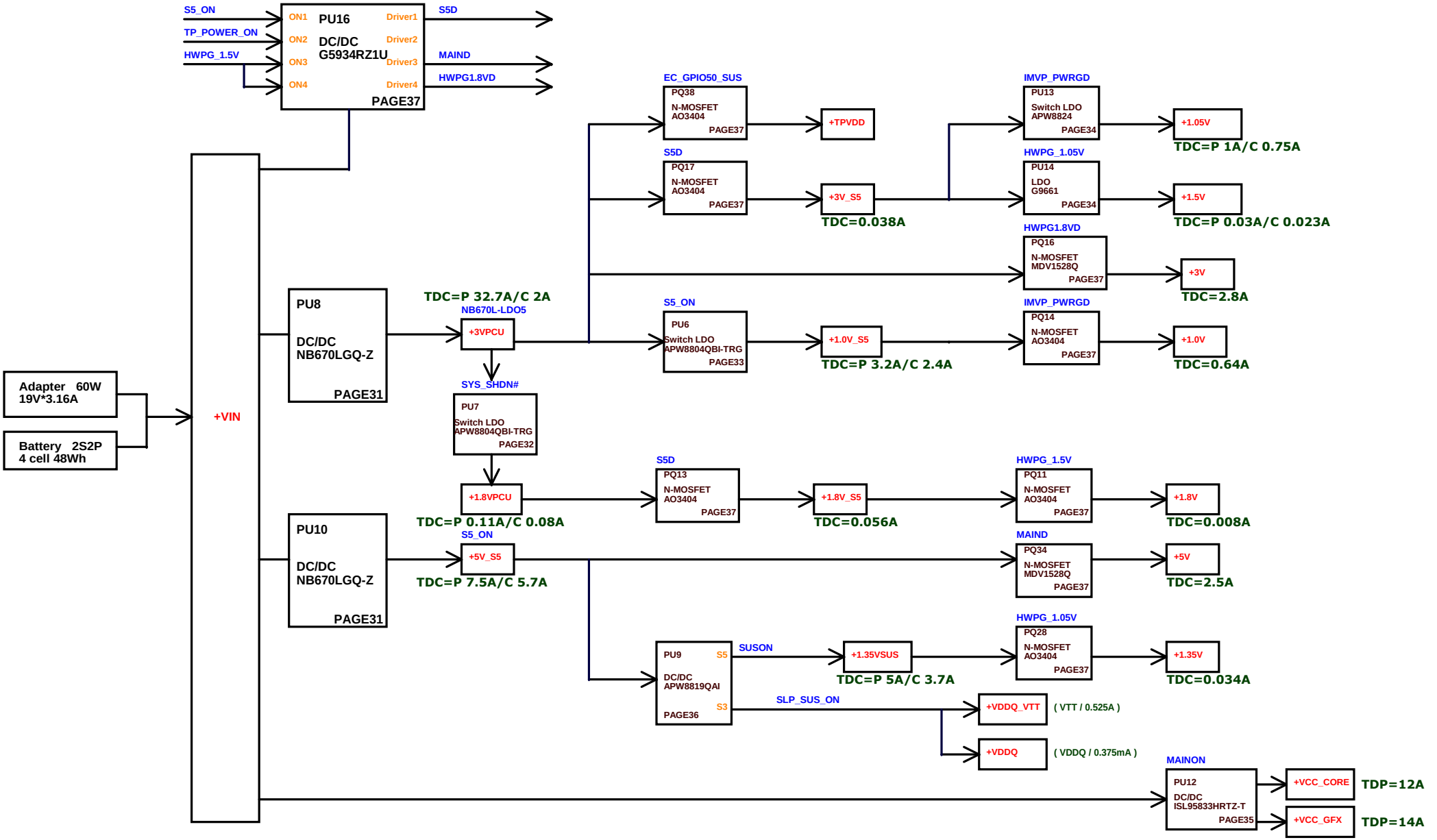
ZYL POWER BLOCK DIAGRAM



Quanta Computer Inc.
PROJECT : ZYL

Size	Document Number	Rev
	ZYL Power Block Diagram	1A

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Model	Date	CHANGE LIST
ZYL REV:A		1. FIRST RELEASED
		Check CPU of P/N. ***Change VRAM of P/N.*** ***Check PJ6 for UMA or Dis- GVA.***
		VGA Chip (Buy and Sell) ***AJ0N15V0T07*** ***VR4GbIII9:*** ***HYNIX Graphic DDRIII 900 4Gb H5TC4G63AFR-11C*** ***AKD5PGWTW13 (B/S)*** ***MICRON Graphic DDRIII 900 4Gb MT41J256M16HA-093G:E*** ***AKD5PZSTL05 (B/S)*** ***SAMSUNG Graphic DDRIII 900 4Gb K4W4G1646D-BC1A*** ***AKD5PGWT504 (B/S)*** CPU (Buy and Sell) Intel Baytrial M cpu n3530 VGA Chip (Buy and Sell) AJ0N15V0T07 VRAM (Buy and Sell) VR2GbIII9 HYNIX Graphic DDRIII 900 2Gb H5TC2G63FFR-11C AKD5MZDTW04 ; AKD5MZDTW05 (B/S) MICRON Graphic DDRIII 900 2Gb MT41J128M16JT-093G:K AKD5MGSTL15 ; AKD5MGSTL25 (B/S) SAMSUNG Graphic DDRIII 900 2Gb K4W2G1646Q-BC1A AKD5MGST511 ; AKD5MGST513 (B/S)
ZYL REV:B	5/27	1.PAGE.22 , modify SW10 pin3 connect to pin1 ,pin2 connect to pin4&pin5&pin6 2.PAGE.24 , modify CN16 & CN18 footprint from "USB-TARA4-9B1323-9P-SMT" to "UB2-UARDM-4K1926-4P-R"
	5/28	1.PAGE.25 , SWAP CN23 USB_CAR_N & USB_CAR_P
	5/29	1.PAGE.40 , Change PR125 from 10K to 26.7K due to 1.05V_GFX output is incorrect
	6/6	1.PAGE.6 , Change C458、C453 from 10P/50V to 12P/50V 2.PAGE.40 , Add PR239 to modify +1.5V_GFX PG sequence
	6/9	1.PAGE.29 , change hole 18、hole20、hole28 footprint from "HG-C315D110P2" to "H-C315D110P2" 2.PAGE.19 , Add D37 D38 C521 3.PAGE.20 , change R66 R67 R69 R70 R71 R73 R74 R76 from 620ohm to 619 ohm 4.PAGE.29 , Change C430 from "CH22206K917" to "CH22206J911" 5.PAGE.22 , Change C464 C466 C468 C469 from "0.01u/16V_4" to "0.01u/25V_4"
	6/10	1.PAGE.29 , reserve & mount C522 C523 C524 for ESD 2.PAGE.40 , Change PL9 from 3.3uH to 2.2uH for modified 1.5V_GFX efficiency.
	6/11	1.PAGE.24 , delete R465 R468 R522 R530 & mount L28,L31 for EMI
	6/13	1.PAGE.7 , PAGE.26,PAGE.28 , unmount R427,C310,R452,R453 2.PAGE.19 , mount D16 and change value form 14V/38V to 5V/30V 3.PAGE.26 , mount C338,C339,C340,C341 for EMI
ZYL REV:C	6/25	1.PAGE.6 , Change G9、G10 footprint from "SOLDERJUMPER-2" to "RC0603-C" 2.PAGE.26 , Change R311、R324、R565、R562、R550、R566 、L23、R13 from "0ohm" to "shortpad"
	6/27	1.PAGE.7 & 28 , Unmount R411 & Delete R147,R148,R149 2.PAGE.9 , Delete R180 for CPU +1.0V voltage
	7/1	1.PAGE.24 & 25 , Change C279,C224,C414 from 100u/6.3V_3216 to 100U/6.3V_3528
	7/2	1.PAGE.38 , Change PR135 from 1.5K/F_4 to 1.91K/F_4 for thermal request
	7/9	1.PAGE.40 , Change PR9 from 54.9K to 64.9K for EMI request and +1.5V_GFX will Change to 1.35V_GFX